US005732014A

United States Patent [19]

Forbes

[11] Patent Number: 5,732,014

[45] Date of Patent: Mar. 24, 1998

[54] **MERGED TRANSISTOR STRUCTURE FOR GAIN MEMORY CELL**

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[21] Appl. No.: **804,179**

[22] Filed: **Feb. 21, 1997**

[51] **Int. Cl.**[6] **G11C 11/24**

[52] **U.S. Cl.** **365/149**; 365/189.04; 365/189.01

[58] **Field of Search** 365/149, 189.04, 365/189.01, 174, 189.09

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[57] **ABSTRACT**

A gain memory cell formed by merged n-channel and p-channel field-effect transistors wherein the body portion of the p-channel transistor is coupled to the charge storage node of the memory cell for providing a bias to the body of the p-channel transistor that varies as a function of the data stored by the memory cell. The stored charge is sensed indirectly in that the stored charge modulates the conductivity of the p-channel transistor so that the p-channel transistor has a first turn-on threshold for a stored logic "1" condition and a second turn-on threshold for a stored logic "0" condition. Consequently, a small storage node capacitance can be used, reducing the overall volume of the cell. The gain memory cell has a single internal contact and only two lines are required for operation of the gain memory cell. The internal contact is formed along a sidewall of an isolation trench, minimizing the surface area of the memory cell.

18 Claims, 7 Drawing Sheets