



US005732014A

**United States Patent** [19]  
**Forbes**

[11] **Patent Number:** **5,732,014**  
[45] **Date of Patent:** **Mar. 24, 1998**

- [54] **MERGED TRANSISTOR STRUCTURE FOR GAIN MEMORY CELL**
- [75] Inventor: **Leonard Forbes**, Corvallis, Oreg.
- [73] Assignee: **Micron Technology, Inc.**, Boise, Id.
- [21] Appl. No.: **804,179**
- [22] Filed: **Feb. 21, 1997**
- [51] Int. Cl.<sup>6</sup> ..... **G11C 11/24**
- [52] U.S. Cl. .... **365/149; 365/189.04; 365/189.01**
- [58] Field of Search ..... **365/149, 189.04, 365/189.01, 174, 189.09**

Ema, T., et al., "3-Dimensional Stacked Capacitor Cell for 16M and 64M DRAMs", *IEDM*, Abstract of Int. Electron Device Meeting, pp. 592-595, (1988).  
 Kim, W., et al., "An Experimental High-Density DRAM Cell with a Built-in Gain Stage", *IEEE Journal of Solid-State Circuits*, vol. 29, No. 8, 978-981, (1994).

(List continued on next page.)

*Primary Examiner*—David C. Nelms  
*Assistant Examiner*—Huan Hoang  
*Attorney, Agent, or Firm*—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

A gain memory cell formed by merged n-channel and p-channel field-effect transistors wherein the body portion of the p-channel transistor is coupled to the charge storage node of the memory cell for providing a bias to the body of the p-channel transistor that varies as a function of the data stored by the memory cell. The stored charge is sensed indirectly in that the stored charge modulates the conductivity of the p-channel transistor so that the p-channel transistor has a first turn-on threshold for a stored logic "1" condition and a second turn-on threshold for a stored logic "0" condition. Consequently, a small storage node capacitance can be used, reducing the overall volume of the cell. The gain memory cell has a single internal contact and only two lines are required for operation of the gain memory cell. The internal contact is formed along a sidewall of an isolation trench, minimizing the surface area of the memory cell.

[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,872,042	10/1989	Maeda et al.	365/149 X
4,970,689	11/1990	Kenney	365/189.01
4,999,811	3/1991	Banerjee	365/149
5,007,002	4/1991	Leigh	365/189.04
5,066,607	11/1991	Banerjee	437/52
5,122,986	6/1992	Lim et al.	365/189.11
5,220,530	6/1993	Itoh	365/189.01
5,308,783	5/1994	Krautschneider et al.	437/52
5,448,513	9/1995	Hu et al.	365/150
5,646,903	7/1997	Johnson	365/189.04
5,652,728	7/1997	Hosotani et al.	365/149 X
5,657,267	8/1997	Levi	365/149

**OTHER PUBLICATIONS**

Cottrell, P., et al., "N-Well Design for Trench DRAM Arrays", *IEEE*, Abstract of Int. Electron Device Meeting, pp. 584-587, (1988).

**18 Claims, 7 Drawing Sheets**

