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Forbes

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[54] **DIFFERENTIAL FLASH MEMORY CELL AND METHOD FOR PROGRAMMING**

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[52] **U.S. Cl.** **365/185.33**; 365/189.01

[58] **Field of Search** 365/185.33, 189.01

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[57] **ABSTRACT**

A flash memory cell. The flash memory cell includes first and second transistors. The first transistor has a control gate coupled to a word line, a drain coupled to a data line and a floating gate. The second transistor, similarly, includes a control gate coupled to the word line, a drain coupled to a second data line and a second floating gate. The first floating gate stores a state of the second transistor prior to programming of the flash memory cell. Further, the second floating gate stores a programmed state of the second transistor. A difference between the states of the first and second transistors represents the value of the data stored in the flash memory cell.

7 Claims, 3 Drawing Sheets