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United States Patent [19]
Forbes

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- [54] **DIFFERENTIAL FLASH MEMORY CELL AND METHOD FOR PROGRAMMING**
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- [52] U.S. Cl. **365/185.33; 365/189.01**
- [58] Field of Search **365/185.33, 189.01**

References Cited

U.S. PATENT DOCUMENTS

5,021,999	6/1991	Kohda et al.	365/168
5,027,171	6/1991	Reedy et al.	357/23.5
5,111,430	5/1992	Marie	365/185
5,253,196	10/1993	Shimabukuro	365/45
5,293,560	3/1994	Harari	365/185
5,317,535	5/1994	Talreja et al.	365/185
5,337,281	8/1994	Kobayashi et al.	365/185.33
5,388,069	2/1995	Kokubo	365/185
5,424,993	6/1995	Lee et al.	365/218
5,430,670	7/1995	Rosenthal	365/45
5,434,815	7/1995	Smarandoiu et al.	365/189.01
5,438,544	8/1995	Makino	365/185
5,467,306	11/1995	Kaya et al.	365/185.2
5,477,485	12/1995	Bergemont et al.	365/185.24
5,485,422	1/1996	Bauer et al.	365/168
5,627,781	5/1997	Hayashi et al.	365/185.2

OTHER PUBLICATIONS

- Alok, D., et al., "Electrical Properties of Thermal Oxide Grown on n-type 6H-Silicon Carbide", *Appl. Phys. Lett.*, vol. 64, 2845-2846, (1994).
- Yu, M. et al., "The Electronic Conduction Mechanism of Hydrogenated Nanocrystalline Silicon Films", *Proc. 4th Int. Conf. on Solid-State and Int. Circuit Tech*, 66-68, (Oct. 1995).

- Bauer, M., et al., "A Multilevel-Cell 32 Mb Flash Memory", *Digest IEEE, Solid-State Circuits Conf.*, 132-133, (1995).
- Boeringer, D.W., et al., "Avalanche amplification of multiple resonant tunneling through parallel silicon microcrystallites", *Physical Rev. B*, vol. 51, 13 337-13 343, (1995).
- Demichelis, F., et al., "Influence of Doping on the Structural and Optoelectronic Properties of Amorphous and Microcrystalline Silicon Carbide", *J. Appl. Phys.*, vol. 72, 1327-1333, (1992).
- Demichelis, F., et al., "Physical Properties of Doped and Undoped Microcrystalline SiC:H Deposited By PECVD", *Symp. on Amorphous Silicon Technology*, vol. 214, 413-418, (1991).

(List continued on next page.)

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[57] **ABSTRACT**

A flash memory cell. The flash memory cell includes first and second transistors. The first transistor has a control gate coupled to a word line, a drain coupled to a data line and a floating gate. The second transistor, similarly, includes a control gate coupled to the word line, a drain coupled to a second data line and a second floating gate. The first floating gate stores a state of the second transistor prior to programming of the flash memory cell. Further, the second floating gate stores a programmed state of the second transistor. A difference between the states of the first and second transistors represents the value of the data stored in the flash memory cell.

7 Claims, 3 Drawing Sheets

