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# United States Patent [19]

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[54] **INTEGRATED CIRCUITS USING OPTICAL FIBER INTERCONNECTS FORMED THROUGH A SEMICONDUCTOR WAFER AND METHODS FOR FORMING SAME**

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[\*] Notice: This patent is subject to a terminal disclaimer.

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[51] Int. Cl.<sup>7</sup> ..... **H01L 21/00**

[52] U.S. Cl. .... **438/31; 438/65; 438/107; 438/456**

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[58] Field of Search ..... 438/29, 31, 455, 438/667, 27, 46, 65, 67, 69, 93, 107, 108, 956; 257/686, 432

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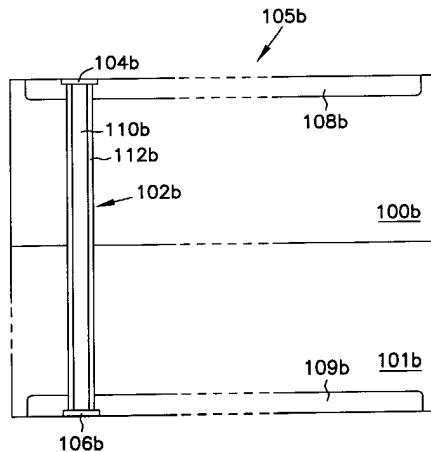
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### [57] ABSTRACT

An integrated circuit with a number of optical fibers that are formed in high aspect ratio holes. The high aspect ratio holes extend through a semiconductor wafer. The optical fibers include a cladding layer and a core formed in the high aspect ratio hole. These optical fibers are used to transmit signals between functional circuits on the semiconductor wafer and functional circuits on the back of the wafer or beneath the wafer.

**22 Claims, 4 Drawing Sheets**



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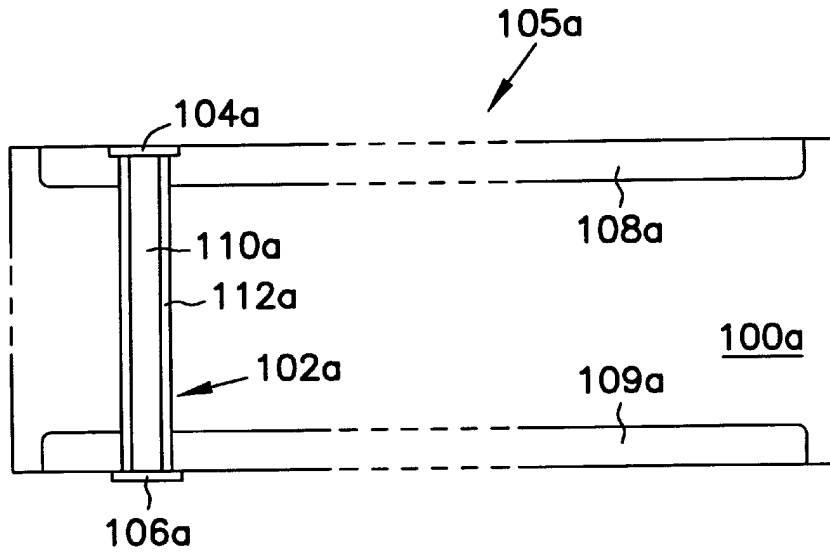


FIG. 1A

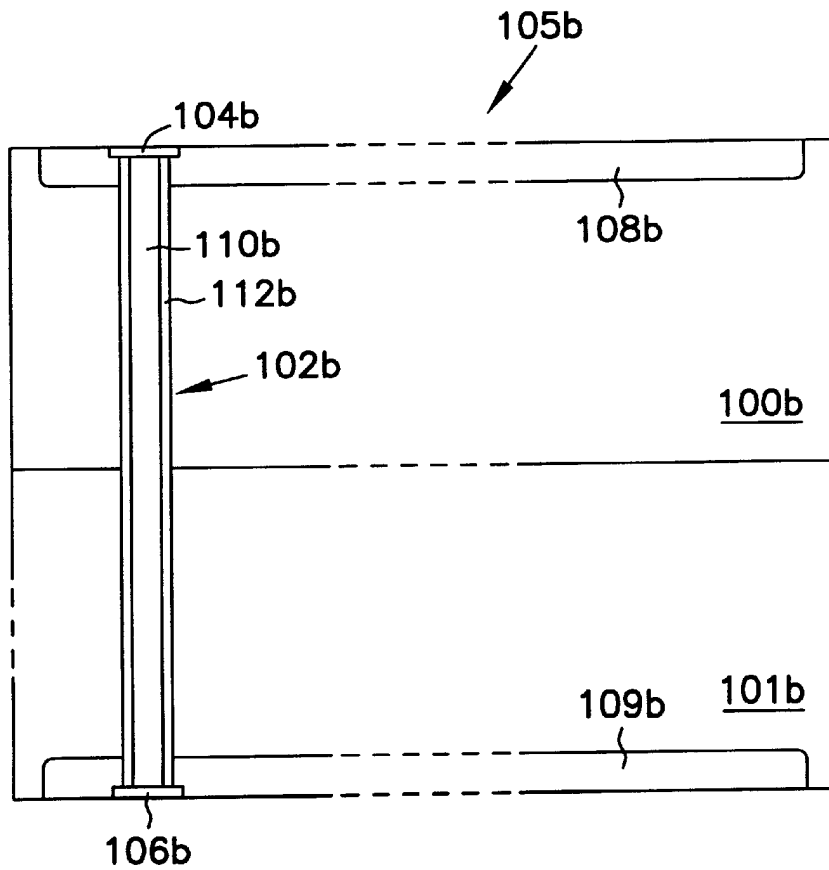
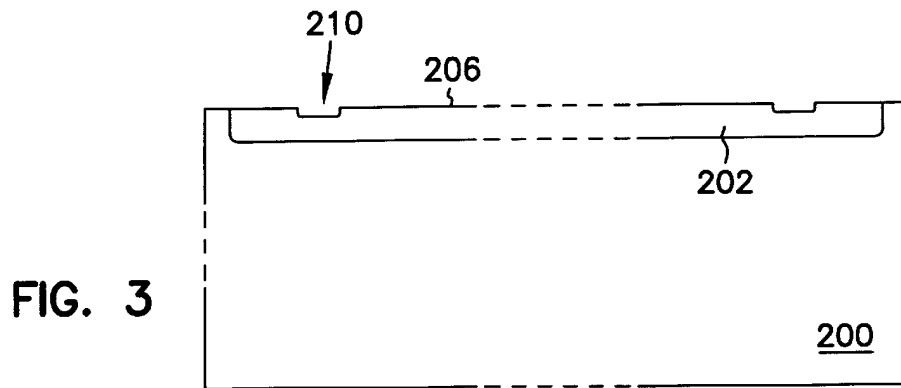
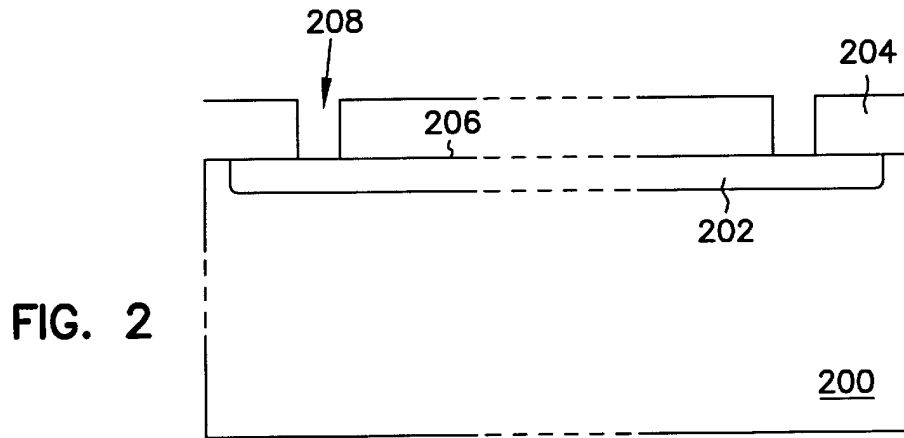
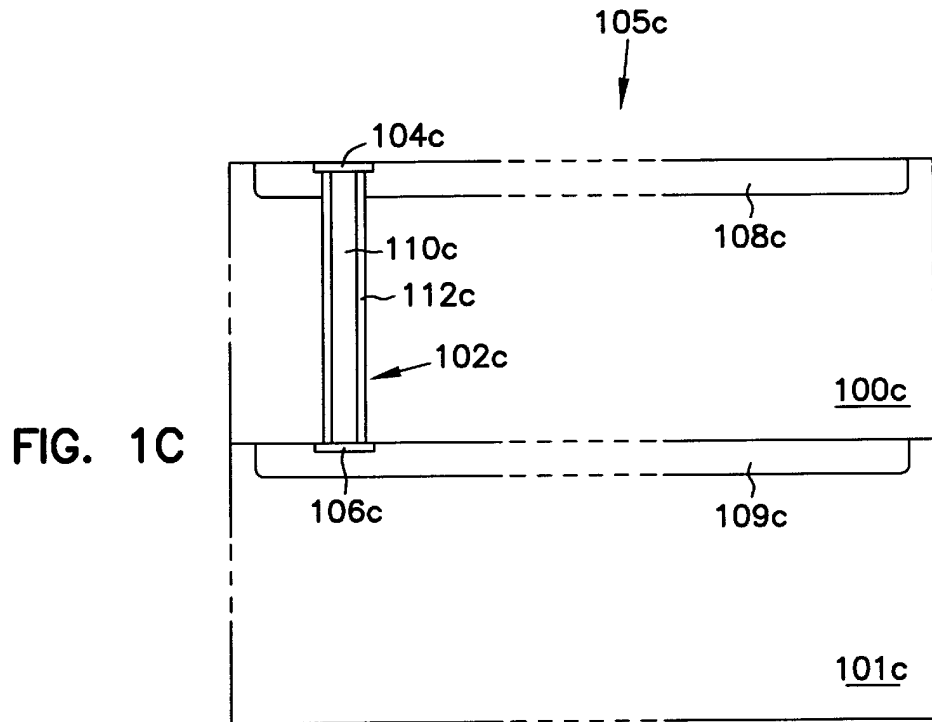
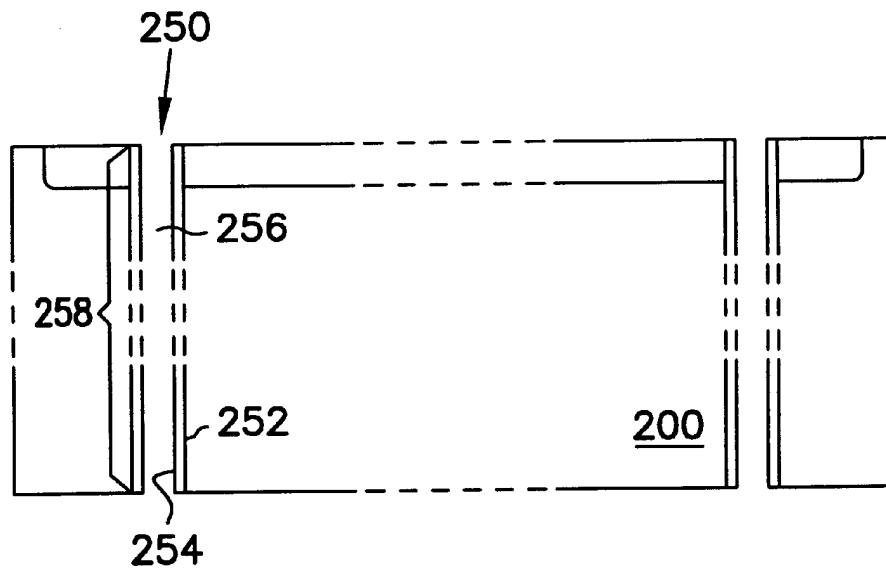
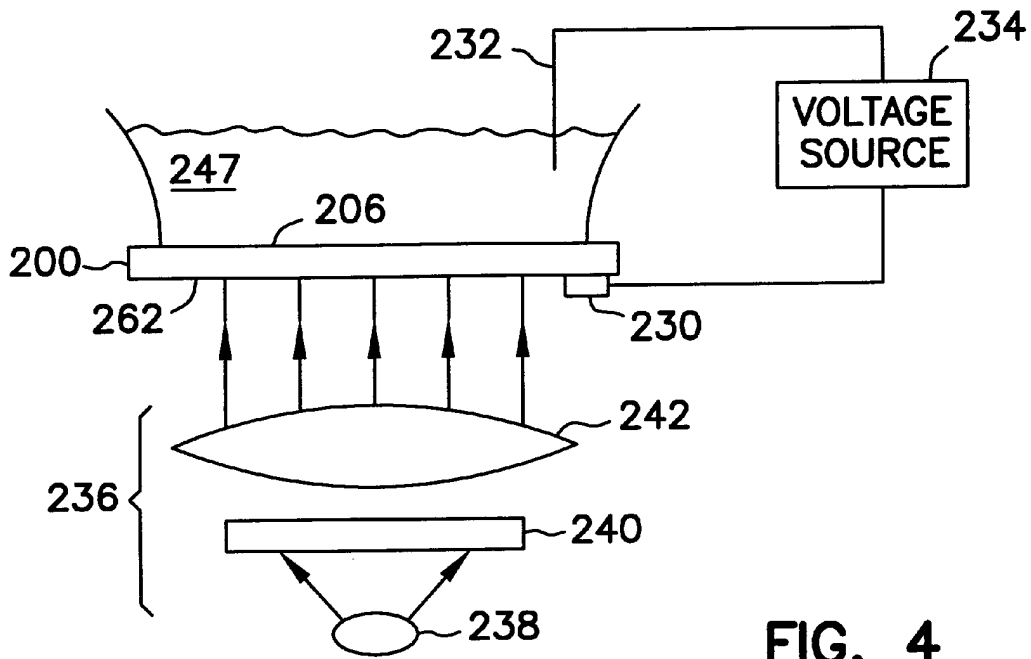


FIG. 1B





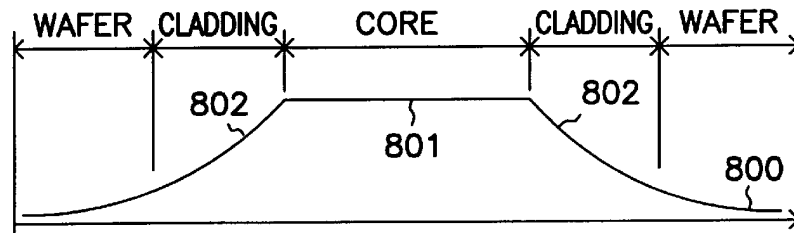
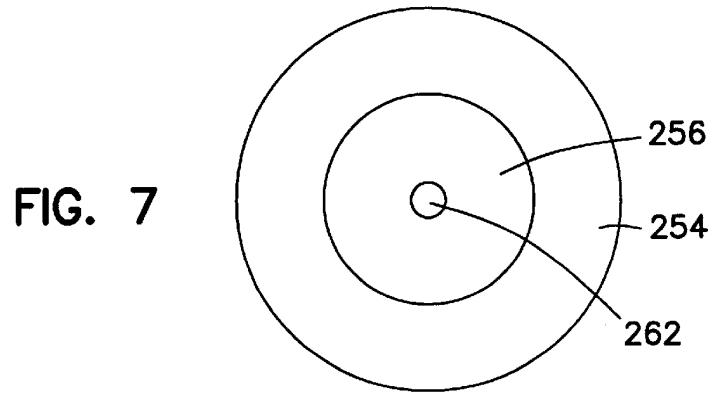
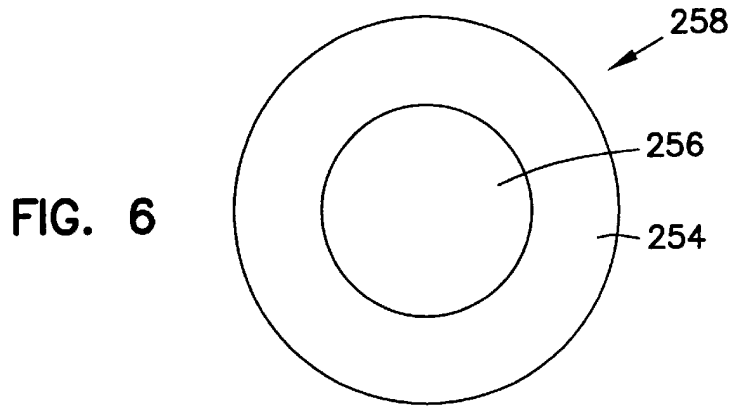


FIG. 8

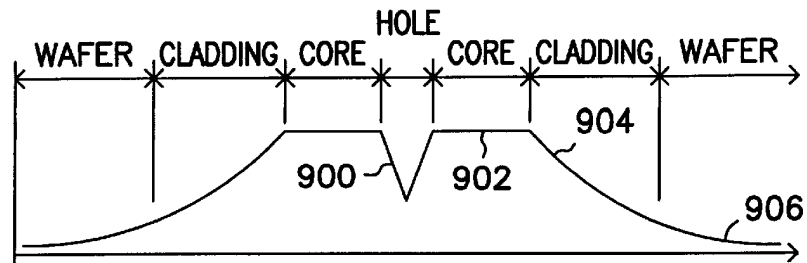


FIG. 9

**INTEGRATED CIRCUITS USING OPTICAL  
FIBER INTERCONNECTS FORMED  
THROUGH A SEMICONDUCTOR WAFER  
AND METHODS FOR FORMING SAME**

**TECHNICAL FIELD OF THE INVENTION**

The present invention relates generally to the field of integrated circuits and, in particular, to integrated circuits using optical fiber interconnects formed through a semiconductor wafer and methods for forming same.

**BACKGROUND OF THE INVENTION**

Electrical systems typically use a number of integrated circuits that are mounted on a printed circuit board. The individual integrated circuits of the system are typically fabricated on different wafers. Each wafer is tested and separated into individual dies or chips. Individual chips are then packaged as individual integrated circuits. Each integrated circuit includes a number of leads that extend from the packaging of the circuit. The leads of the various integrated circuits, are interconnected to allow information and control signals to be passed between the integrated circuits such that the system performs a desired function. For example, a personal computer includes a wide variety of integrated circuits, e.g., a microprocessor and memory chips, that are interconnected on one or more printed circuit boards in the computer.

While printed circuit boards are useful for bringing together separately fabricated and assembled integrated circuits, the use of printed circuit boards creates some problems which are not so easily overcome. For example, printed circuit boards consume a large amount of physical space compared to the circuitry of the integrated circuits which are mounted to them. It is desirable to reduce the amount of physical space required by such printed circuit boards. Further, assuring the electrical integrity of interconnections between integrated circuits mounted on a printed circuit board is a challenge. Moreover, in certain applications, it is desirable to reduce the physical length of electrical interconnections between devices because of concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

A continuing challenge in the semiconductor industry is to find new, innovative, and efficient ways of forming electrical connections with and between circuit devices which are fabricated on the same and on different wafers or dies. Relatedly, continuing challenges are posed to find and/or improve upon the packaging techniques utilized to package integrated circuitry devices. As device dimensions continue to shrink, these challenges become even more important.

For reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for an improved technique for interconnecting individual integrated circuits in an electronic system.

**SUMMARY OF THE INVENTION**

The above mentioned problems with integrated circuits and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Integrated circuits are described which use optical fibers that extend through the thickness of a semiconductor substrate or wafer so as to allow communication between integrated circuits formed on opposite sides of a

single wafer, on opposite sides of two wafers that are bonded together, formed on wafers in a stack that are bonded together, or other appropriate configuration of wafers.

In one embodiment, a method for interconnecting first and second integrated circuits is provided. The first integrated circuit is formed on a working surface of a first semiconductor substrate. At least one high aspect ratio hole is formed through the first semiconductor substrate. An optical fiber with a cladding layer and a core is formed in the at least one high aspect ratio hole. The optical fiber having first and second ends. The first integrated circuit is coupled to the second integrated circuit through the optical fiber. In one embodiment, the second integrated circuit is formed on a second surface of the first semiconductor substrate, opposite the working surface of the first semiconductor substrate. In another embodiment, the second integrated circuit is formed on a working surface of a second semiconductor substrate. The second semiconductor substrate is bonded to the first semiconductor substrate such that the first and second integrated circuits are coupled together through the optical fiber in the first semiconductor substrate. In another embodiment, the surfaces of the first and second semiconductor substrates that are bonded together are located on sides of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates, respectively.

In another embodiment, an electronic system is provided. The electronic system includes at least one semiconductor wafer. A number of integrated circuits are also provided. At least one integrated circuit is formed on the at least one semiconductor wafer. The at least one semiconductor wafer includes at least one optical fiber formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer. At least one optical transmitter and at least one optical receiver are associated with the at least one optical fiber. The optical transmitter and optical receiver transmit optical signals between selected integrated circuits of the electronic system over the optical fiber.

In another embodiment, an integrated circuit is provided. The integrated circuit includes a functional circuit formed on a wafer. A number of optical fibers are formed in high aspect ratio holes that extend through the wafer. The optical fibers include a cladding layer and a center core that are formed from materials with different indices of refraction.

In another embodiment, a method for forming an integrated circuit in a semiconductor wafer with an optical fiber that extends through the semiconductor wafer is provided. The method includes forming a functional circuit in a first surface of the semiconductor wafer. A number of etch pits are formed in the first surface of the semiconductor wafer at selected locations in the functional circuit. An anodic etch of the semiconductor wafer is performed such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface. A cladding layer of an optical fiber is formed on an inner surface of the high aspect ratio holes. A core layer of the optical fiber is also formed. The optical fiber is selectively coupled to the functional circuit.

In another embodiment, a method for forming an optical fiber through a semiconductor substrate is provided. The method includes forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface. A cladding layer of an optical fiber is formed on an inner surface of the at least one high aspect ratio hole. A core layer of the optical fiber

is also formed. In one embodiment, the cladding layer comprises an oxide layer formed in the high aspect ratio holes. In another embodiment, the core layer comprises a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer. In another embodiment, the core layer comprises a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A, 1B, and 1C are elevational views of exemplary embodiments of an integrated circuit with a semiconductor wafer having an optical fiber formed in an high aspect ratio hole that extends through the semiconductor wafer according to the teachings of the present invention.

FIGS. 2, 3, 4, 5, 6, and 7 are views of a semiconductor wafer at various points of an illustrative embodiment of a method for forming an integrated circuit with optical fibers formed through at least one semiconductor wafer according to the teachings of the present invention.

FIGS. 8 and 9 are graphs that show guided waves in optical fibers according to the teachings of the present invention.

#### DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific illustrative embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

FIG. 1A is an elevational view of an embodiment of the present invention. Electronic system **105a** includes semiconductor wafer **100a**. Semiconductor wafer **100a** includes at least one optical fiber **102a** that provides a path for transmitting signals between functional circuit **108a** on a first surface of semiconductor wafer **100a** and functional circuit **109a** on a second, opposite surface of semiconductor wafer **100a**. It is noted that a number of optical fibers can be formed through semiconductor wafer **100a**.

Optical fiber **102a** is formed in a high aspect ratio hole in semiconductor wafer **100a**. The high aspect ratio hole is formed using, for example, an anodic etching technique as described in more detail below. Typically, the high aspect ratio holes have an aspect ratio in the range of approximately 100 to 200. Conventionally, a semiconductor wafer has a thickness in the range of approximately 100 to 1000 microns. Thus, the high aspect ratio holes used to form the optical fibers can be fabricated with a width that is in the range from approximately 0.5 microns to approximately 10 microns.

Optical fiber **102a** is coupled to functional circuits **108a** and **109a**. For example, optical transmitter **104a** is coupled to one end of optical fiber **102a** and optical receiver **106a** is coupled to a second, opposite end of optical fiber **102a**. Optical transmitter **104a** is also coupled to a node of functional circuit **108a** and optical receiver **106a** is coupled to a node of functional circuit **109a**. In one embodiment, optical transmitter **104a** comprises a gallium arsenide transmitter that is bonded to the first surface of semiconductor wafer **100a** using conventional wafer bonding techniques. In this embodiment, optical receiver **106a** comprises a silicon photodiode detector formed in the second surface of semiconductor wafer **100a**. In other embodiments, other appropriate optical receivers and transmitters may be used to transmit signals over optical fiber **102a**.

Optical fiber **102a** comprises cladding layer **112a** that separates core **110a** from semiconductor wafer **100a**. In this structure, semiconductor wafer **100a** acts as the outer "sheath" for optical fiber **102a**. Various materials can be used to form core **110a** and cladding layer **112a**. Basically, core **110a** comprise a material with a higher index of refraction than the material of cladding layer **112a** and thus provides normal optical fiber waveguide characteristics. Specific examples of materials for core **110a** and cladding layer **112a** are provided below with respect to FIGS. 6 and 7.

Since the optical fiber is formed in a wafer of semiconductor material, absorption by and radiation in the semiconductor wafer can affect the operation of the optical fiber. For example, if the wavelength of the light transmitted in optical fiber **102a** is greater than the absorption edge of the semiconductor wafer, e.g., 1.1 microns for silicon, then semiconductor wafer **100a** will not absorb the light transmitted in optical fiber **102a**. However, due to the large change in index of refraction at the interface between cladding layer **112a** and semiconductor wafer **100a**, some radiation loss occurs into semiconductor wafer **100a**. This case is depicted, for example, in FIG. 8.

FIG. 8 is a graph that illustrates the magnitude of the radiation in optical fiber **102a** along a diameter of optical fiber **102a**. In the region of core **256**, indicated at **801**, optical waves are guided with no substantial loss along the length of optical fiber **102a**. Evanescent fields are present in the region of cladding layer **254** as indicated at **802**. These evanescent fields drop off to insignificant levels as indicated at **800** in the surrounding semiconductor wafer.

In the case of shorter wavelength light transmitted in optical fiber **102a**, there will be some absorption as well as radiation into the semiconductor substrate. For example, with a silicon wafer, light with a wavelength of less than 1.1 microns produces some small losses due to absorption and radiation into the silicon wafer.

In some cases, it is advantageous to limit the penetration of the optical wave into semiconductor wafer **100a**. This avoids problems related to possible photoregeneration of

carriers in the surrounding semiconductor wafer **100a** that might interfere with the normal operation of other integrated circuitry. To prevent optical waves from penetrating the semiconductor wafer, the hole that houses the optical fiber can be lined with a reflecting metal mirror prior to forming the cladding layer. A technique for forming the metal layer is described in co-pending application Ser. No. 09/031,961, entitled Integrated Circuits Using Optical Waveguide Interconnects Formed Through a Semiconductor Wafer and Methods for Forming Same, which application is incorporated by reference.

Optical fibers can be added to circuits using a conventional layout for the circuit without adversely affecting the surface area requirements of the circuit. Conventional circuits typically include pads formed on the top surface of the semiconductor wafer that are used to connect to leads of the integrated circuit through bonding wires. Advantageously, the bonding wires of conventional circuits can be replaced by optical fibers **102a** to allow signals to be passed between various integrated circuits of electronic system **105a** without the need to attach the individual integrated circuits to a printed circuit board. This allows a substantial space savings in the design of electrical systems along with overcoming concerns related to signal loss or dissipation and interference with and by other integrated circuitry devices in the electrical system.

FIGS. 1B and 1C show additional embodiments of electronic systems using optical fibers formed through integrated circuits to interconnect various integrated circuits. In the embodiment of FIG. 1B, integrated circuits **108b** and **109b** are formed in working surfaces of semiconductor wafers **100b** and **101b**. Surfaces opposite the working surfaces of semiconductor wafers **100b** and **101b** are bonded together using conventional wafer bonding techniques. Optical fiber **102b** transmits signals between integrated circuits **108b** and **109b**. A portion of optical fiber **102b** is formed in each of the semiconductor wafers **100b** and **101b**. In the embodiment of FIG. 1C, semiconductor wafers **100c** and **101c** are stacked with the working surface of semiconductor wafer **101c** beneath the surface of semiconductor wafer **100c** that is opposite the working surface of semiconductor wafer **100c**. In this embodiment, optical fiber **102c** is formed within semiconductor wafer **100c**.

FIGS. 2, 3, 4, 5, 6, and 7 are views of semiconductor wafer **200** at various points of an illustrative embodiment of a method for forming optical fibers through a semiconductor wafer according to the teachings of the present invention. Functional circuit **202** is formed in an active region of semiconductor wafer **200**. For purposes of clarity, the Figures only show the formation of two optical fibers through semiconductor wafer **200**. However, it is understood that with a particular functional circuit any appropriate number of optical fibers can be formed. Essentially, the optical fibers are formed in the same space on the surface of semiconductor wafer **200** that is conventionally used to form bonding pads for leads. In a conventional circuit, the leads of the integrated circuit are connected to a printed circuit board which routes signals to other integrated circuits. The optical fibers advantageously remove the need for a printed circuit board to interconnect the functional circuits formed on individual semiconductor wafers.

As shown in FIG. 2, photo resist layer **204** is formed on surface **206** of semiconductor substrate **200**. Photo resist layer **204** is patterned to provide openings **208** at points on surface **206** where high aspect ratio holes are to be formed through semiconductor wafer **200**.

As shown in FIG. 3, etch pits **210** are formed by standard alkaline etching through openings **208** in photo resist layer **204**. Photo resist layer **204** is then removed.

FIG. 4 is a schematic diagram that illustrates an embodiment of a layout of equipment used to carry out an anodic etch that is used to form high aspect ratio holes **250** of FIG. 5. Typically, holes **250** have an aspect ratio in the range of 100 to 200. Bottom surface **262** of semiconductor wafer **200** is coupled to voltage source **234** by positive electrode **230**. Further, negative electrode **232** is coupled to voltage source **234** and is placed in a bath of 6% aqueous solution of hydrofluoric acid (HF) on surface **206** of semiconductor wafer **200**.

In this example, illumination equipment **236** is also included because semiconductor wafer **200** is n-type semiconductor material. When p-type semiconductor material is used, the illumination equipment is not required. Illumination equipment **236** assures that there is a sufficient concentration of holes in semiconductor wafer **200** as required by the anodic etching process. Illumination equipment **236** includes lamp **238**, IR filter **240**, and lens **242**. Illumination equipment **236** focuses light on surface **262** of semiconductor wafer **200**.

In operation, the anodic etch etches high aspect ratio holes through semiconductor wafer **200** at the location of etch pits **210**. Voltage source **234** is turned on and provides a voltage across positive and negative electrodes **230** and **232**. Etching current flows from surface **206** to positive electrode **230**. This current forms the high aspect ratio holes through semiconductor wafer **200**. Further, illumination equipment illuminates surface **262** of semiconductor wafer **200** so as to assure a sufficient concentration of holes for the anodic etching process. The size and shape of the high aspect ratio holes through semiconductor wafer **200** depends on, for example, the anodization parameters such as HF concentration, current density, and light illumination. An anodic etching process is described in V. Lehmann, *The Physics of Macropore Formation in Low Doped n-Type Silicon*, J. Electrochem. Soc., Vol. 140, No. 10, pp. 2836–2843, October 1993, which is incorporated herein by reference.

As shown in FIG. 5, cladding layer **254** is formed on surface **252** of high aspect ratio holes **250**. Further, core **256** is formed within hole **250** such that cladding layer **254** and core **256** comprise optical fiber **258**.

Core **256** has an index of refraction that is greater than the index of refraction of cladding layer **254**. Cladding layer **254** may comprise, for example, a transparent dielectric film such as silicon oxide ( $\text{SiO}_2$ ), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), a nitride, other oxide, or other appropriate dielectric material. Cladding layer **254** is deposited with a uniformity that allows light to be transmitted through optical fiber **258** with normal optical fiber waveguide characteristics. When a nitride is used, cladding layer **254** can be deposited with the required uniformity using the technique described in K. P. Muller, et al, *Trench Node Technology for Gigabit DRAM Generations*, 1996 IEDM Technical Digest, p. 507–510 which is incorporated by reference. This technique allows nitride films to be deposited at low temperatures and low deposition rates to insure uniform coverage of very deep trenches. A technique referred to as “atomic layer epitaxy” can also be used to deposit cladding layer **254**. Atomic layer epitaxy has been described for use with the deposition of silicon oxide ( $\text{SiO}_2$ ). See J. W. Klaus, et al, *Atomic Layer Controlled Growth of  $\text{SiO}_2$  Films Using Binary Reaction Sequence Chemistry*, *Appl. Phys. Lett.* 70(9), Mar. 3, 1997, pp. 1092–1094, which is incorporated by reference. Further, atomic layer epitaxy has been described for use with deposition of aluminum oxide ( $\text{Al}_2\text{O}_3$ ). The atomic layer epitaxy technique deposits material with a thickness of 1 to 2

angstroms for a single binary reaction sequence. Thus, the technique advantageously allows the high aspect ratio holes that house the optical fibers to be lined with a uniform cladding layer.

In one embodiment, optical fiber **258** transmits light with a wavelength that is greater than 1.1 microns. In this embodiment, cladding layer **254** comprises silicon oxide ( $\text{SiO}_2$ ) with an index of refraction of approximately 1.5 or aluminum oxide ( $\text{Al}_2\text{O}_3$ ) with an index of refraction of approximately 1.7. Core **256** comprises lightly doped polysilicon. The lightly doped polysilicon has an index of refraction of approximately 3.4 and exhibits low optical absorption at wavelengths of greater than 1.1 microns. Optical fiber **258** of this embodiment is shown in cross section in FIG. 6.

In another embodiment, cladding layer **254** comprises silicon oxide ( $\text{SiO}_2$ ) and core **256** comprises an oxide or nitride with a higher index of refraction, e.g., aluminum oxide ( $\text{Al}_2\text{O}_3$ ). A cross section of optical fiber **258** of this embodiment is shown in FIG. 7. Core **256** does not completely fill the center of optical fiber **258**. Hole **262** extends along the length of core **256** through semiconductor wafer **200**. However, as long as hole **262** has a diameter that is less than 0.59 times the wavelength of the light transmitted over optical fiber **258**, the light will still be guided by core **256** as shown in FIG. 9. This embodiment can transport light with a wavelength that is less than 1.1 microns. This allows a gallium arsenide emitter to be used at one end of optical fiber **258** to transmit signals down optical fiber **258** and a simple silicon photodiode detector to be used as the receiver on the opposite end of optical fiber **258**.

FIG. 9 is a graph that illustrates the magnitude of the radiation in an optical fiber of the type shown in FIG. 7 along a diameter of the optical fiber. In the region of hole **262**, an evanescent field is present as indicated at **900**. In the region of core **256**, radiation in the optical fiber is guided along the length of the fiber without significant loss in intensity. Evanescent fields are present in the region of cladding layer **254** as indicated at **904**. These evanescent fields drop off to insignificant levels as indicated at **906** in the surrounding semiconductor wafer.

### CONCLUSION

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, other materials such as oxides, nitrides, or high index glasses can be used to form the cladding layer and the core of an optical fiber that extends through a semiconductor wafer. It is noted that optical fibers **102** and **258** can transmit signals in either direction through the semiconductor wafer by proper placement of transmitters and receivers. Further, electronic systems can include more than two semiconductor wafers with sufficient optical fibers formed through the semiconductor wafers to allow signals to be communicated between the integrated circuits of the various semiconductor wafers.

Advantageously, using optical fibers according to the teachings of the present invention allows electronic systems to be constructed in less physical space compared to conventional electronic systems by removing the need for large printed circuit boards to interconnect various integrated circuits. This also provides the advantage of reducing the

cost of packaging integrated circuits for a particular electronic system by allowing a number of circuits to be packaged together. Further, using the optical fibers assures the electrical integrity of interconnections between integrated circuits by reducing the physical length of electrical interconnections between devices. This reduces concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

What is claimed is:

1. A method for interconnecting first and second integrated circuits, wherein the first integrated circuit is formed on a working surface of a first semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the first semiconductor substrate;

forming an optical fiber with a cladding layer and a core in the at least one high aspect ratio hole, the optical fiber having first and second ends; and

coupling the first integrated circuit to the second integrated circuit through the optical fiber.

2. The method of claim 1, and further comprising forming the second integrated circuit on a second surface, opposite the working surface of the first semiconductor substrate.

3. The method of claim 1, and further comprising:

forming the second integrated circuit in a working surface of a second semiconductor substrate; and

bonding the first and second semiconductor substrates together such that the first and second integrated circuits are coupled together through the optical fiber in the first semiconductor substrate.

4. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding surfaces of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates.

5. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding a working surface of the second semiconductor substrate with a surface of the first semiconductor substrate that is opposite the working surface of the first semiconductor substrate.

6. The method of claim 1, wherein forming at least one high aspect ratio hole comprises:

forming etch pits at selected locations in the first surface of the semiconductor substrate; and

performing an anodic etch of the first semiconductor substrate such that high aspect ratio holes are formed through the first semiconductor substrate at the location of the etch pits.

7. The method of claim 1, wherein coupling the first integrated circuit to the second integrated circuit comprises forming optical transmitters and receivers on opposite ends of the optical fiber so as to transmit signals between the first and second integrated circuits.

8. The method of claim 7, wherein forming an optical transmitter comprises forming a gallium arsenide optical transmitter that is bonded to a surface of the first semiconductor substrate and forming an optical receiver comprises forming a silicon photodiode detector at an opposite end of the optical fiber.

9. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of  $\text{SiO}_2$  and forming a core of polysilicon.

10. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of  $\text{Al}_2\text{O}_3$  and forming a core of polysilicon.

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11. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer of  $\text{SiO}_2$  and forming a core of  $\text{Al}_2\text{O}_3$ .

12. The method of claim 1, wherein forming the optical fiber comprises forming a core with a hole that runs substantially along the center of the optical fiber wherein the hole has a diameter that is less than 0.59 times the wavelength of the light to be transmitted in the optical fiber.

13. The method of claim 1, wherein forming the optical fiber comprises forming a cladding layer that surrounds a core layer, wherein the core layer has an index of refraction that is greater than the index of refraction of the cladding layer.

14. The method of claim 1, wherein forming the optical fiber comprises forming the cladding layer using atomic layer epitaxy.

15. A method for forming an integrated circuit in a semiconductor wafer with an optical fiber that extends through the semiconductor wafer, the method comprising:

forming a functional circuit in a first surface of the semiconductor wafer;

forming a number of etch pits in the first surface of the semiconductor wafer at selected locations in the functional circuit;

performing an anodic etch of the semiconductor wafer such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface;

forming a cladding layer of an optical fiber on an inner surface of the high aspect ratio holes;

forming a core layer of the optical fiber; and selectively coupling the optical fiber to the functional circuit.

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16. The method of claim 15, wherein forming a cladding layer comprises forming an oxide layer in the high aspect ratio holes.

17. The method of claim 15, wherein forming the core layer comprises forming a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer.

18. The method of claim 15, wherein forming the core layer comprises forming a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

19. A method for forming an optical fiber through a semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface;

forming a cladding layer of an optical fiber on an inner surface of the at least one high aspect ratio hole; and

forming a core layer of the optical fiber.

20. The method of claim 19, wherein forming a cladding layer comprises forming an oxide layer in the high aspect ratio holes.

21. The method of claim 19, wherein forming the core layer comprises forming a layer of an oxide with an index of refraction that is greater than the index of refraction of the cladding layer.

22. The method of claim 19, wherein forming the core layer comprises forming a layer with a hole that extends substantially along the length of the optical fiber with a diameter that is less than 0.59 times the wavelength of light used to transmit signals over the optical fiber.

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