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Noble et al.

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(54) **PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS**

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(51) **Int. Cl.**⁷ **H03K 19/177**

(52) **U.S. Cl.** **326/41; 326/102**

(58) **Field of Search** 257/302, 202,
257/330, 320; 326/39, 41, 44, 101, 102

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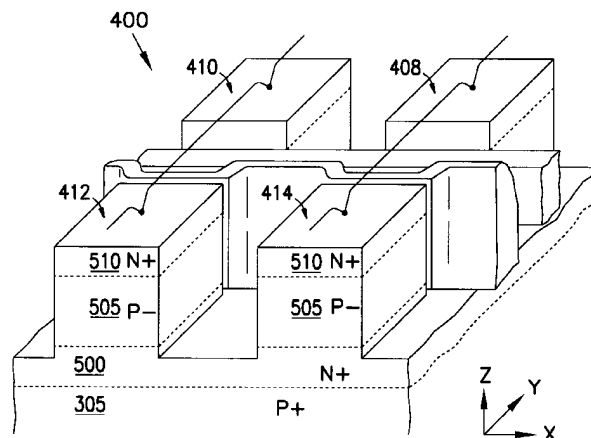
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(57) **ABSTRACT**

A programmable logic array is provided. The programmable logic array includes first and second logic planes. The first logic plane receives a number of input signals. The first logic plane includes a plurality of vertical transistors arranged in rows and columns that are interconnected to provide a number of logical outputs. The second logic plane also includes a number of vertical transistors arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function.

30 Claims, 12 Drawing Sheets



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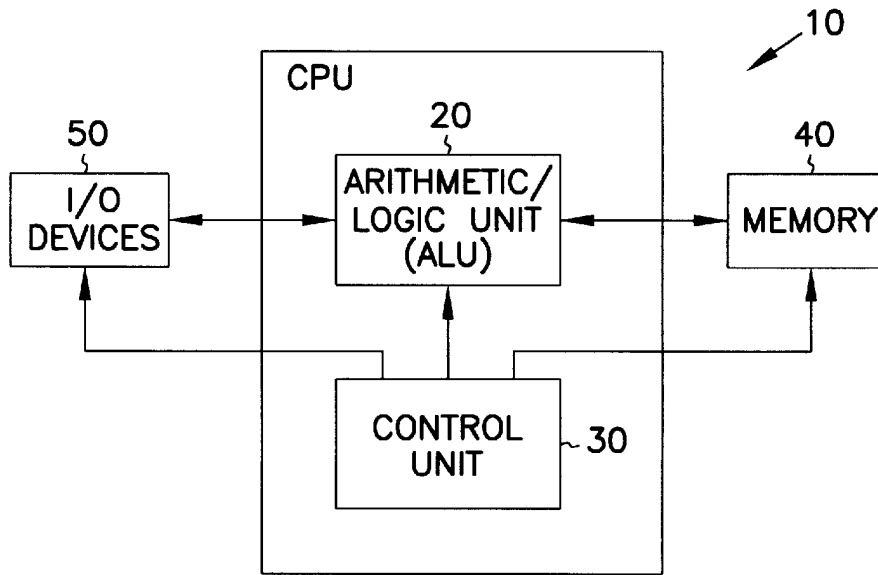


FIG. 1

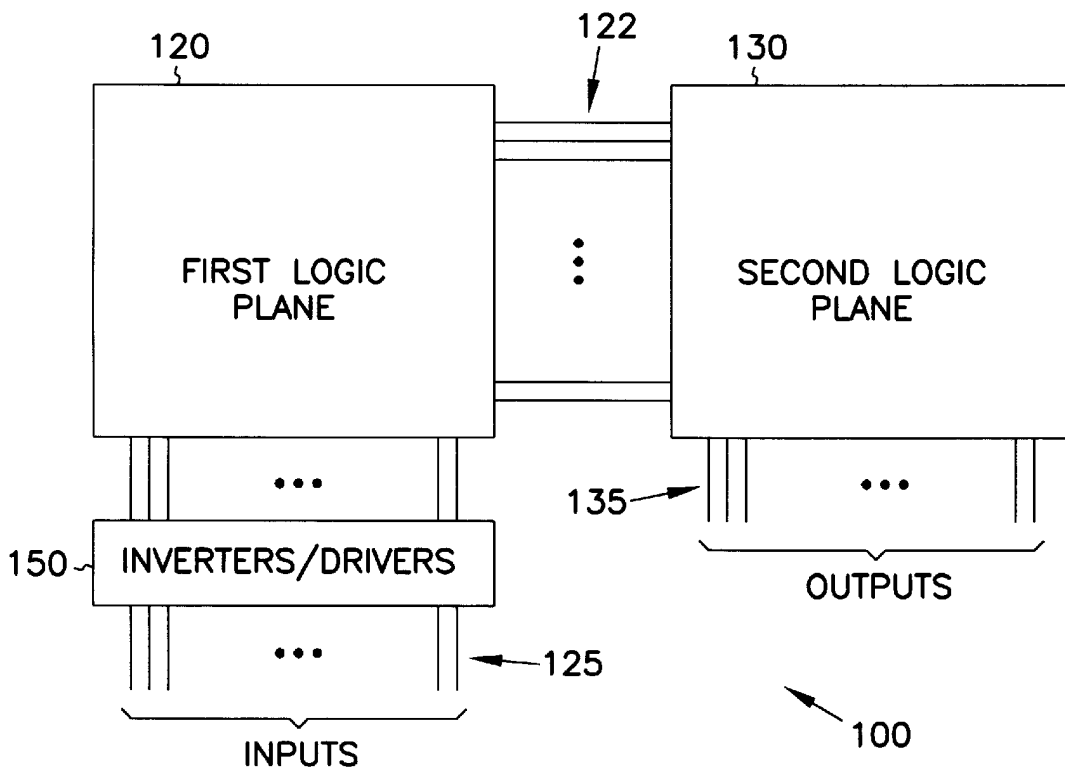


FIG. 2

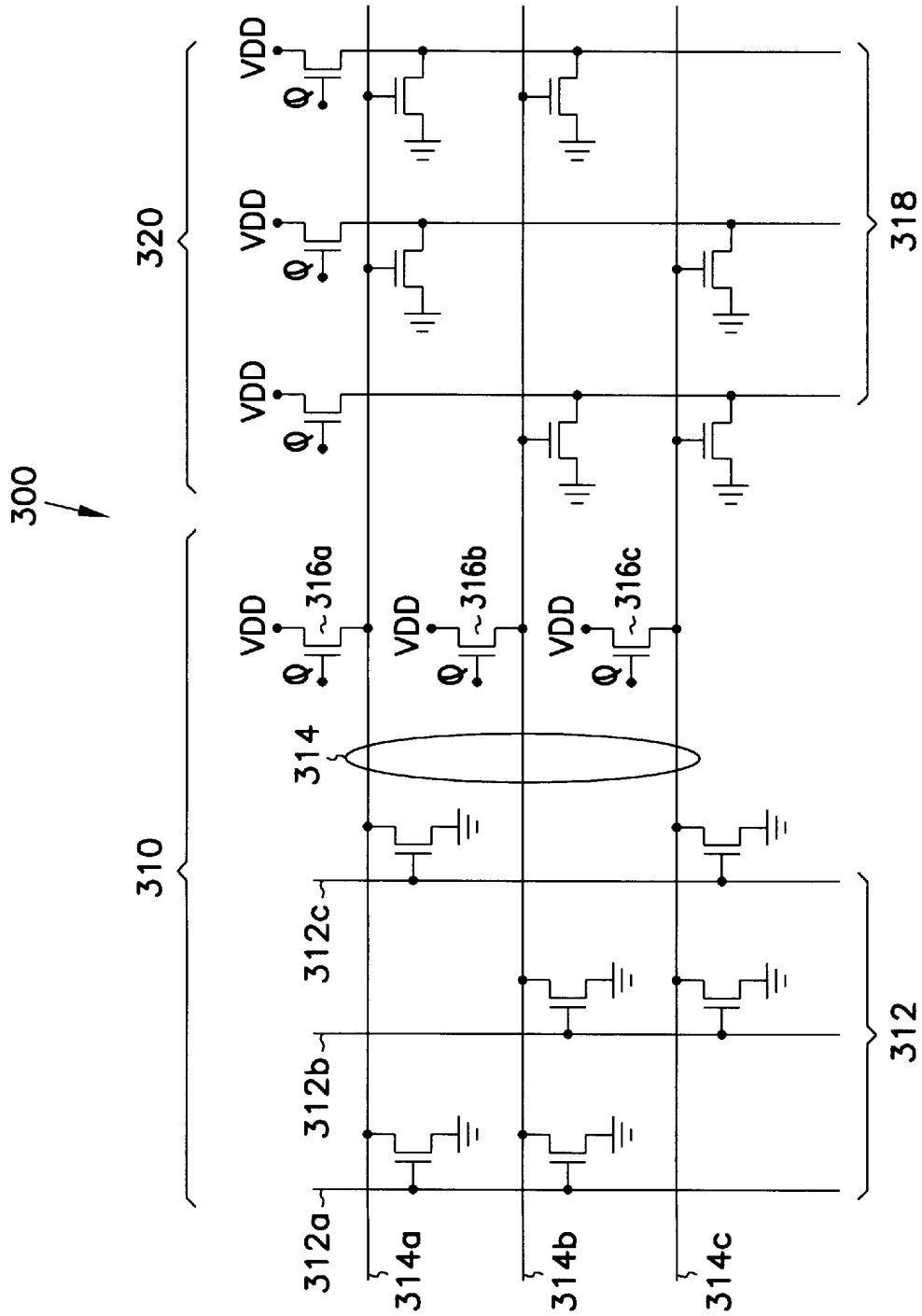


FIG. 3

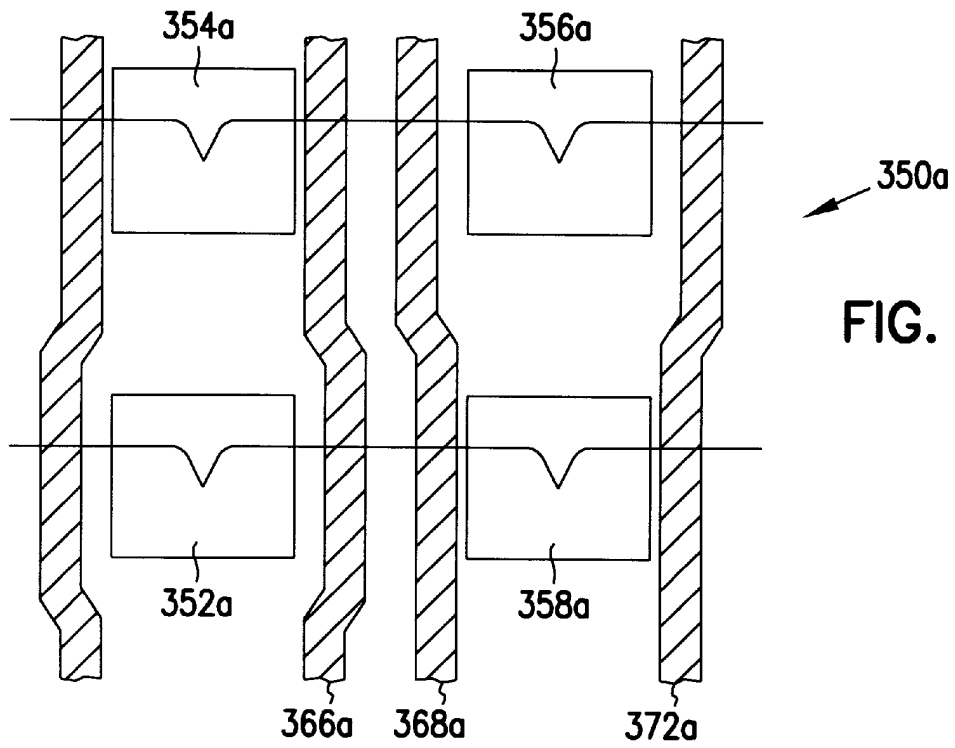


FIG. 4

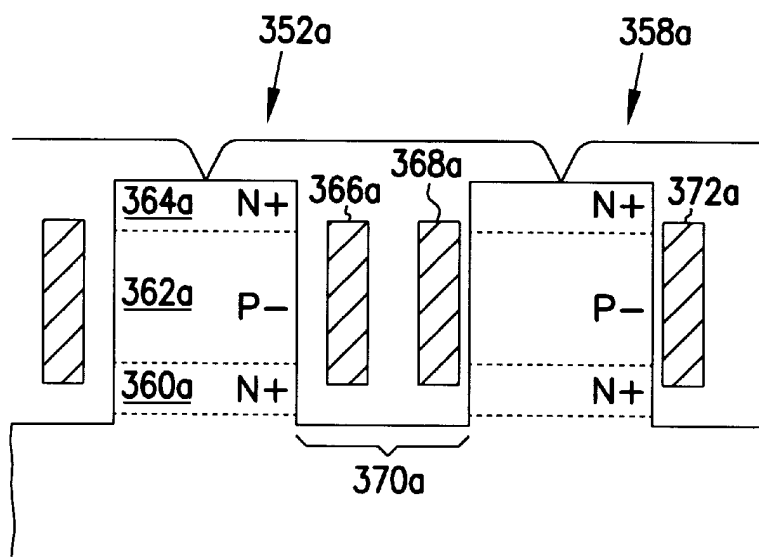
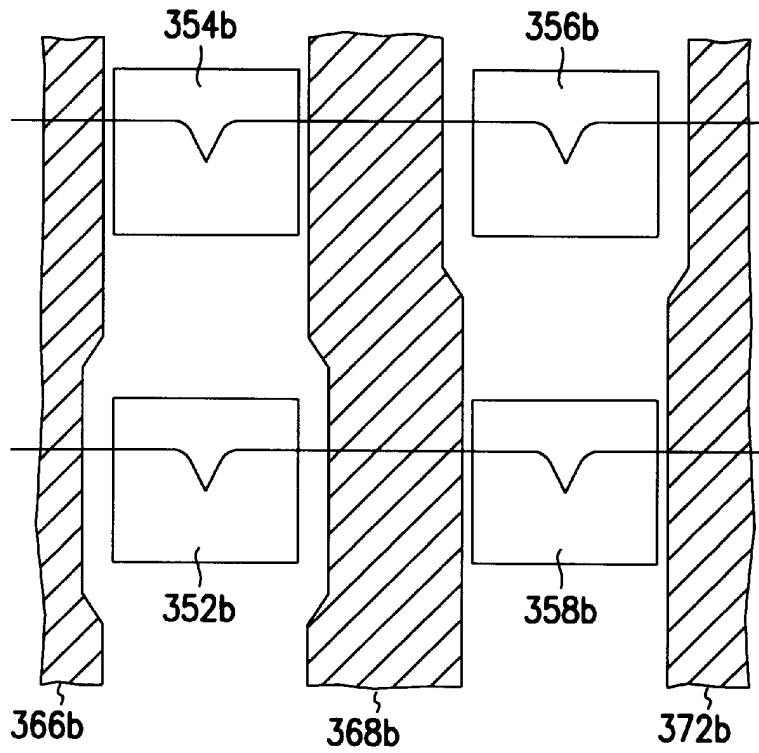


FIG. 5



350b

FIG. 6

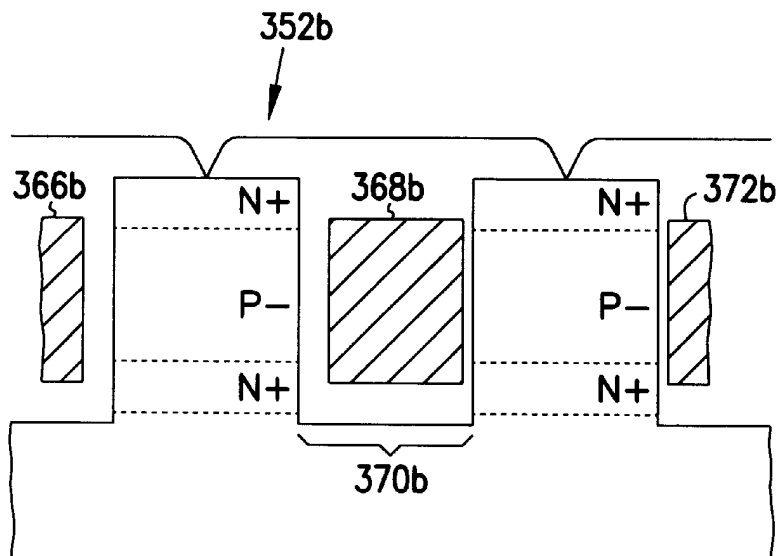


FIG. 7

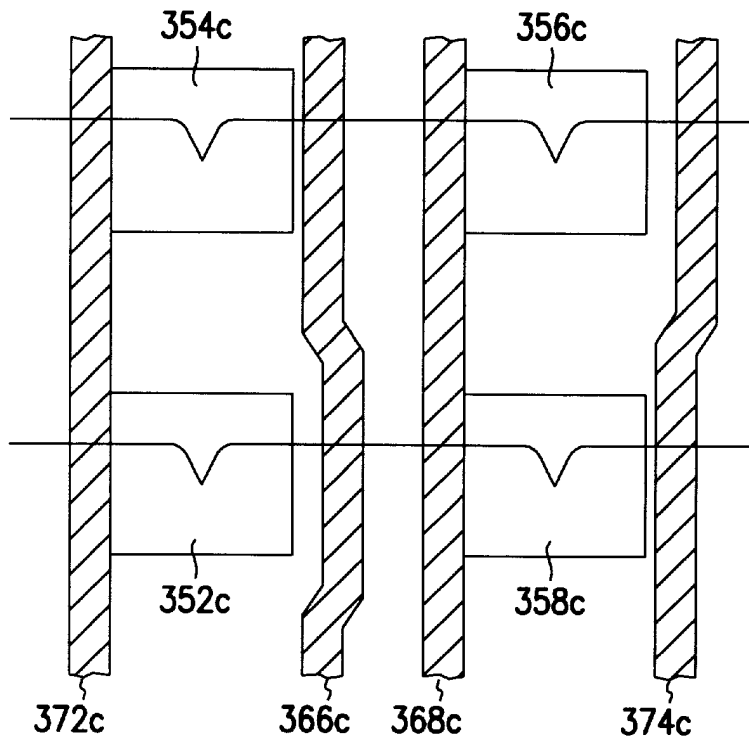


FIG. 8

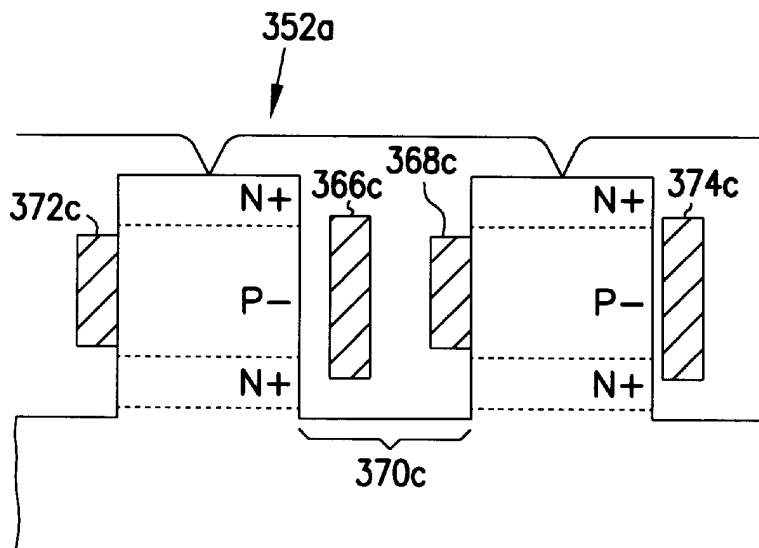


FIG. 9

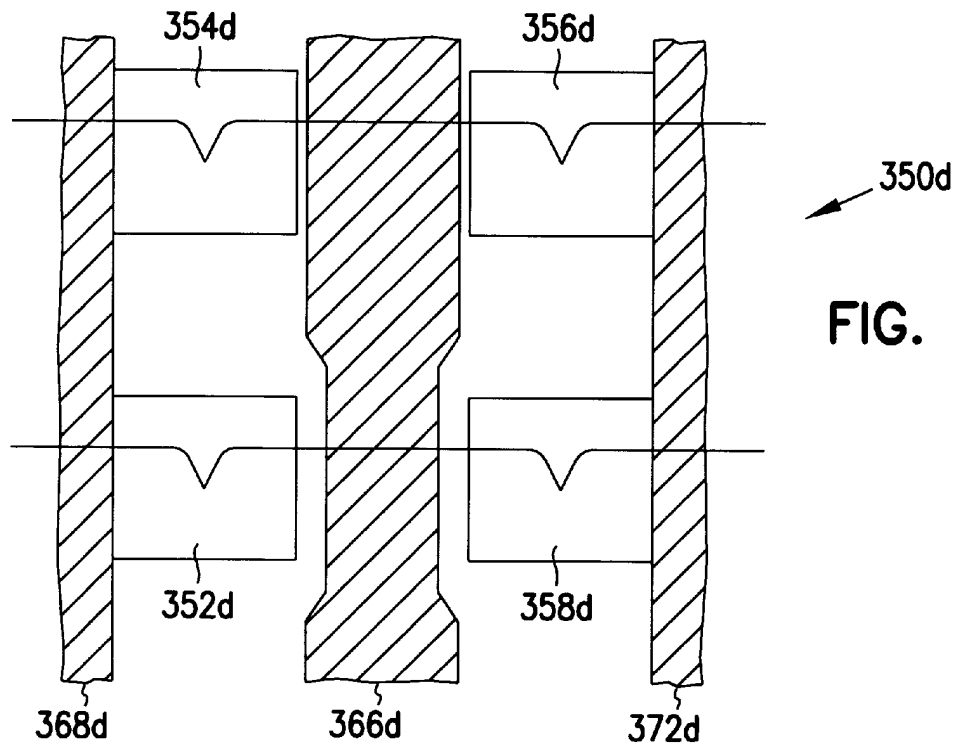


FIG. 10

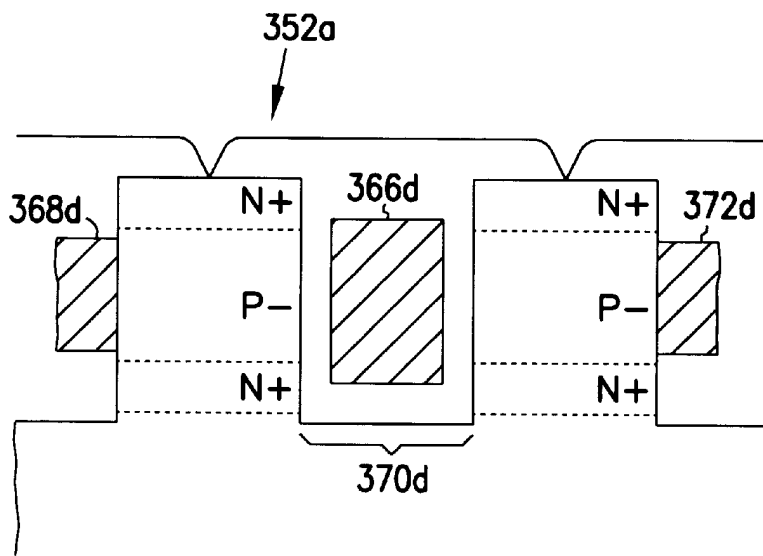


FIG. 11

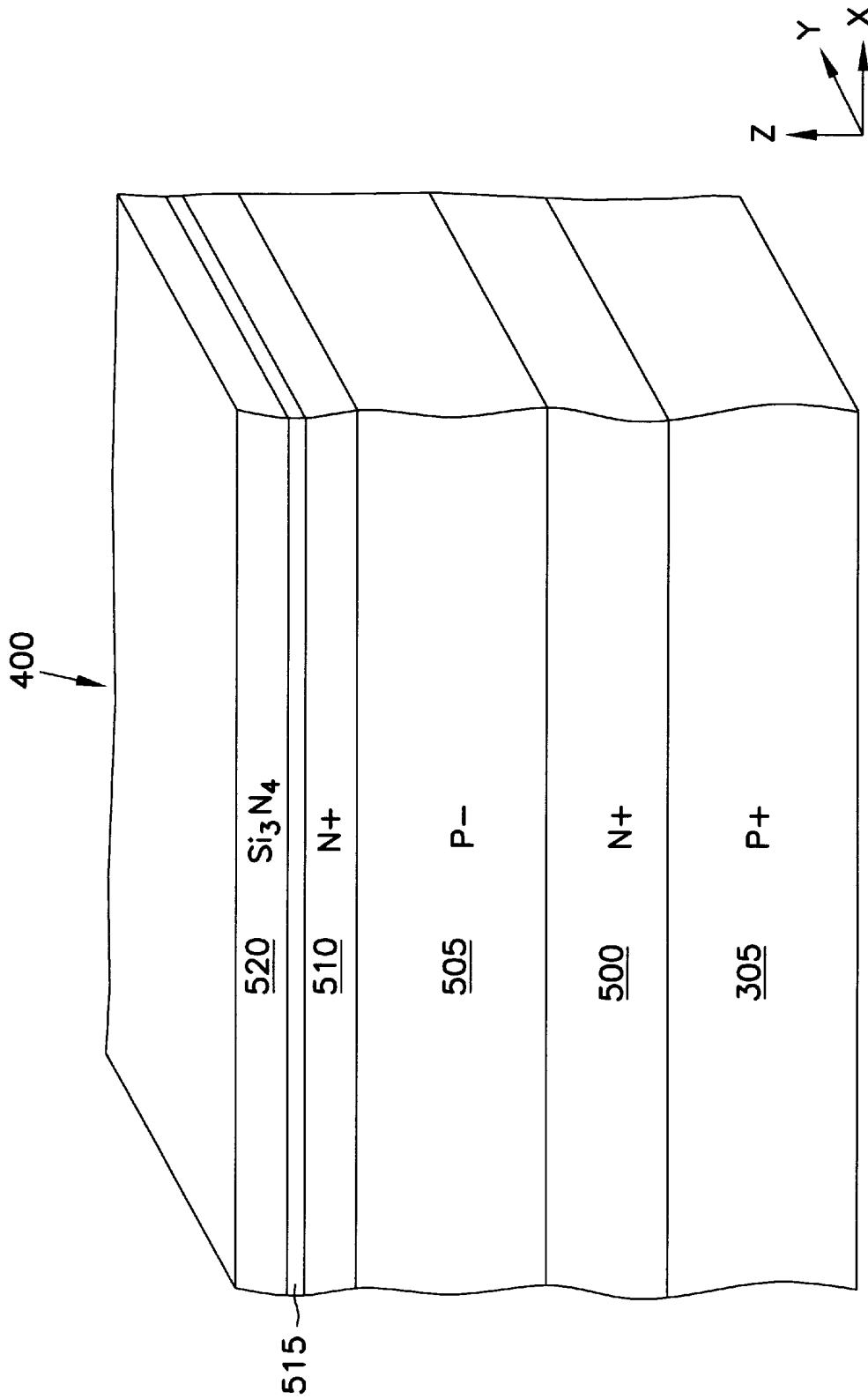
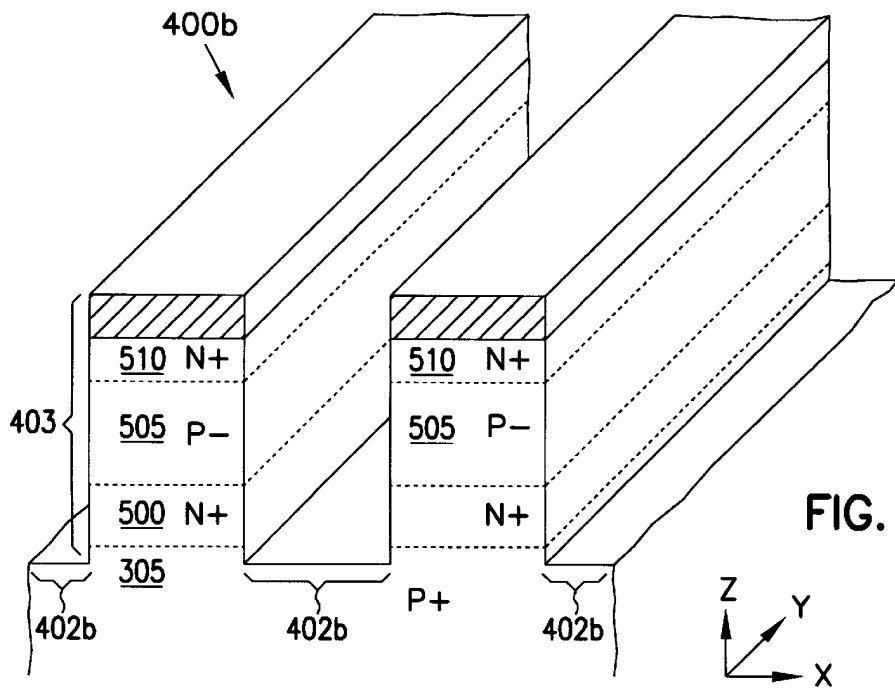
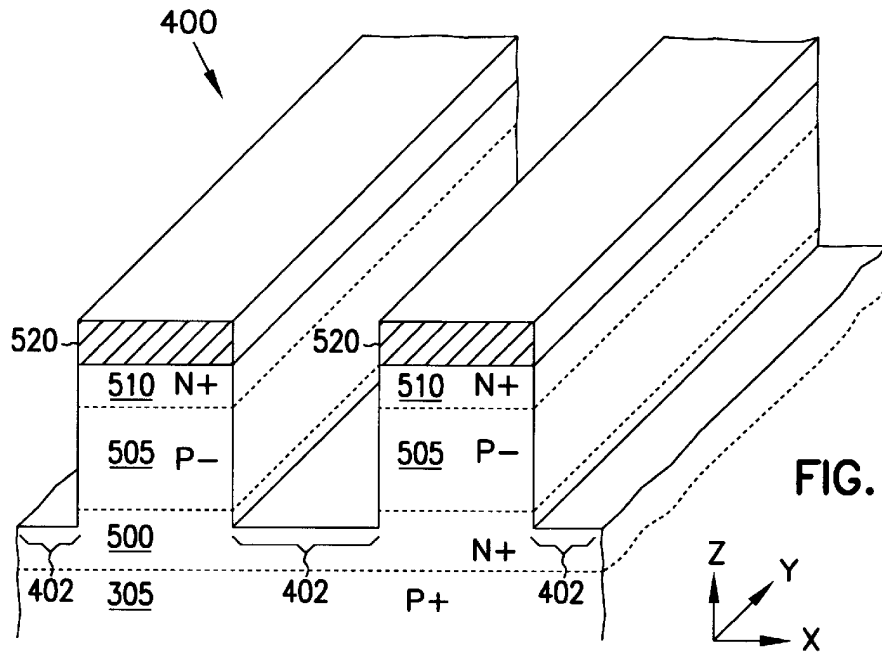


FIG. 12



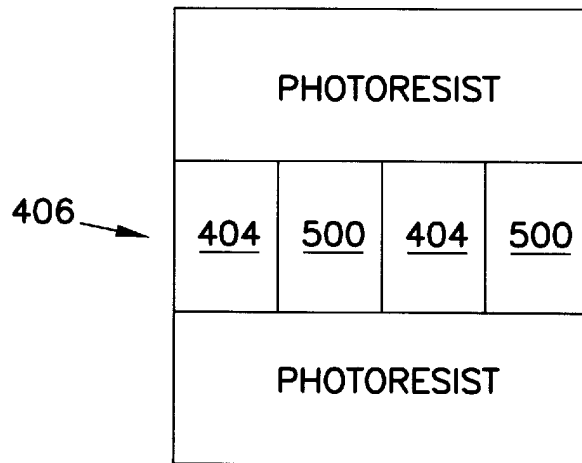


FIG. 14

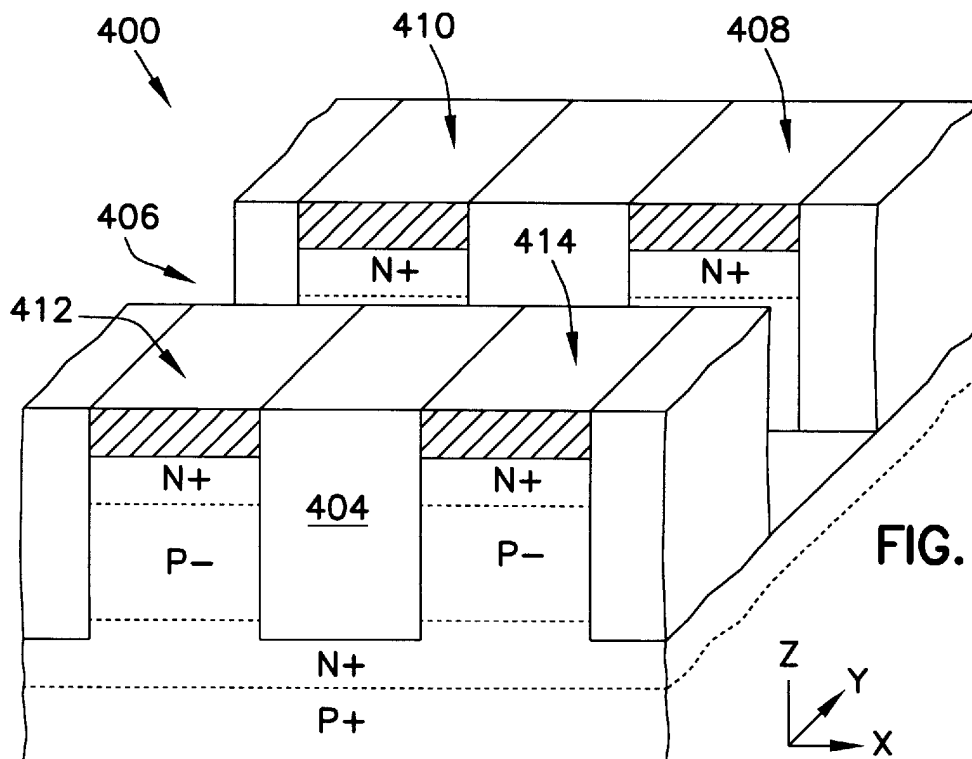


FIG. 15

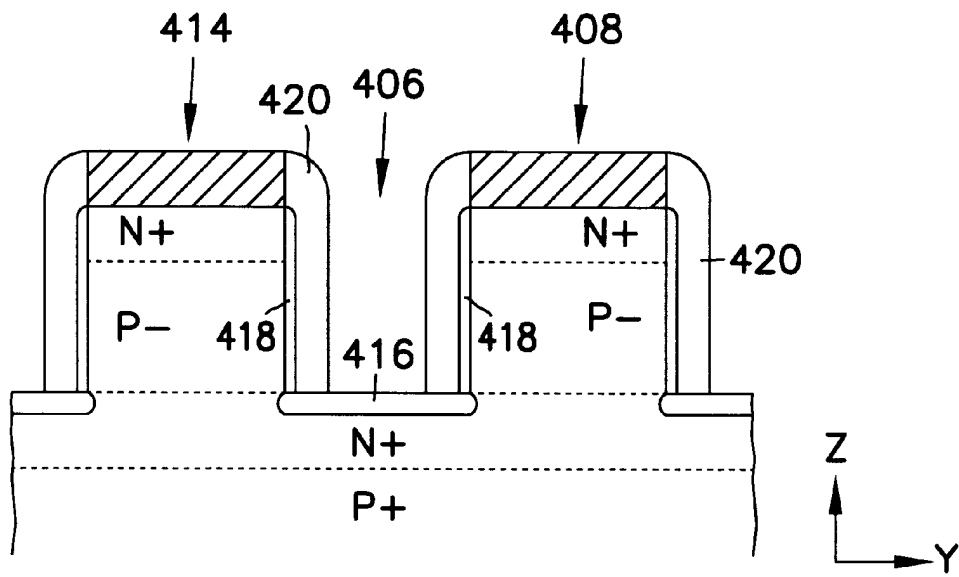


FIG. 16

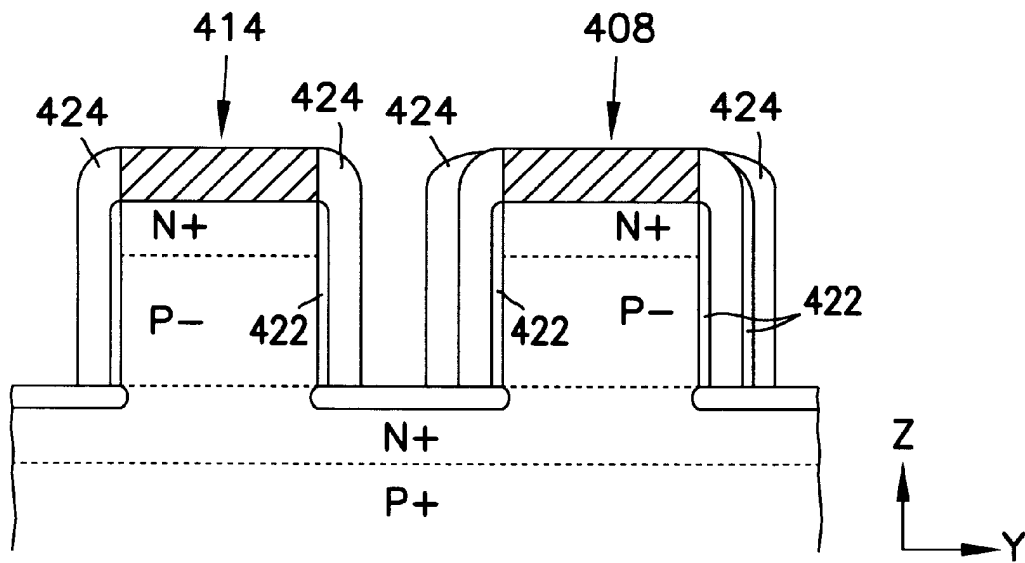


FIG. 17

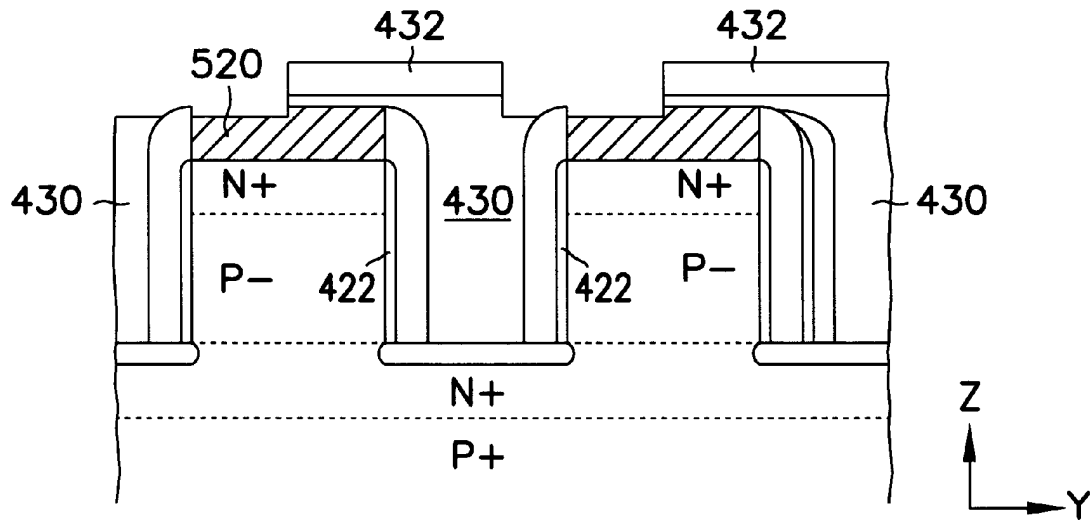


FIG. 18

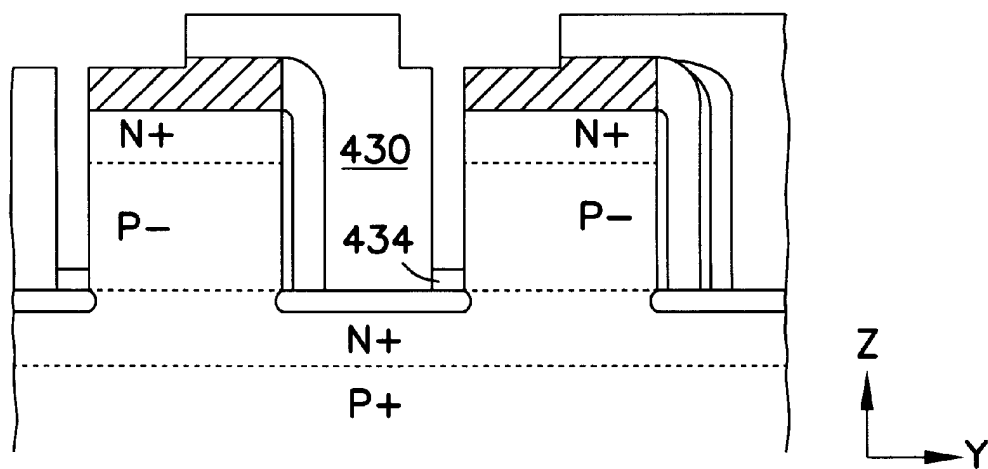


FIG. 19

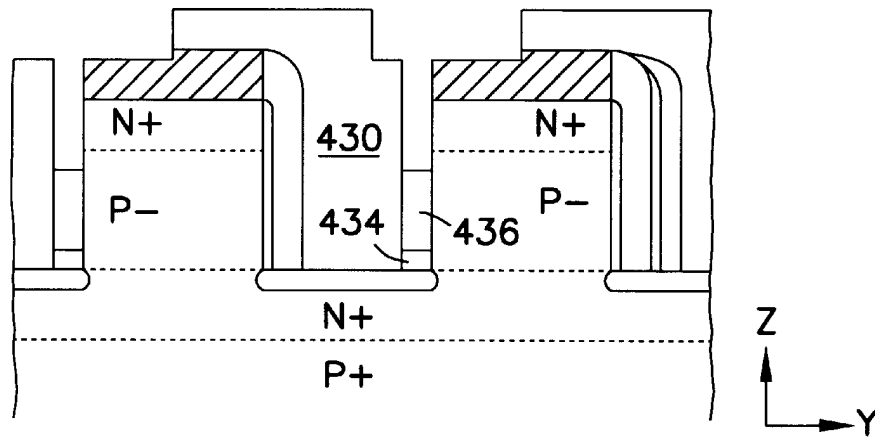


FIG. 20

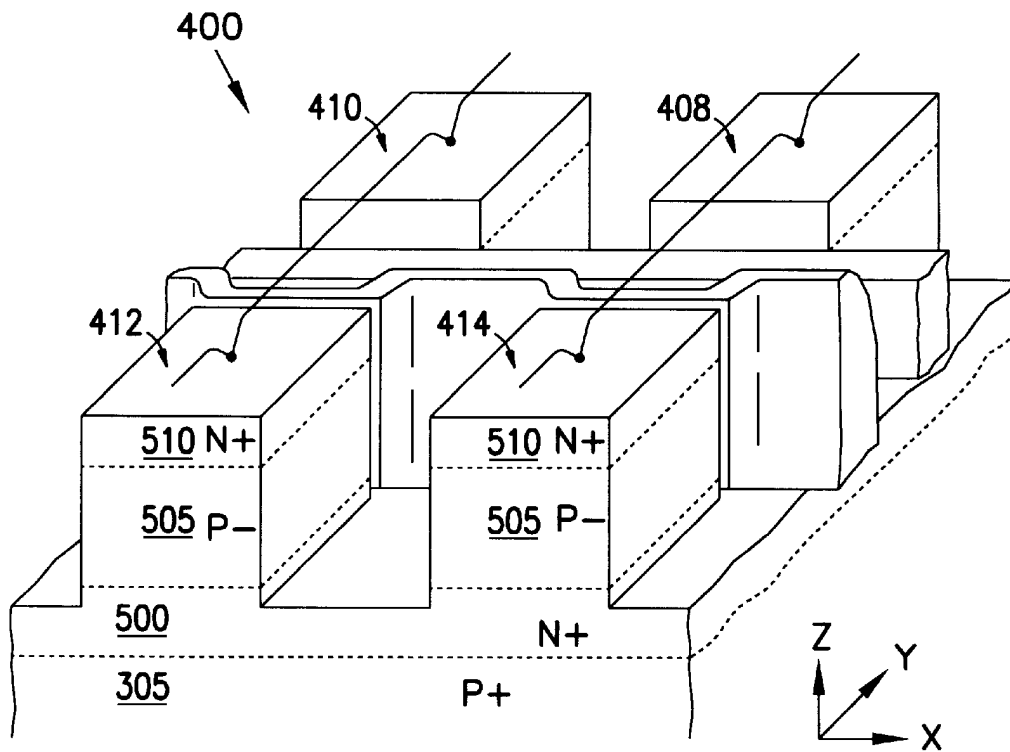


FIG. 21

PROGRAMMABLE LOGIC ARRAY WITH VERTICAL TRANSISTORS

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and in particular to a programmable logic array with vertical transistors.

BACKGROUND OF THE INVENTION

Logic circuits are an integral part of digital systems, such as computers. Essentially, a logic circuit processes a number of inputs to produce a number of outputs for use by the digital system. The inputs and outputs are generally electronic signals that take on one of two "binary" values, a "high" logic value or a "low" logic value. The logic circuit manipulates the inputs using binary logic which describes, in a mathematical way, a given or desired relationship between the inputs and the outputs of the logic circuit.

Logic circuits that are tailored to the specific needs of a particular customer can be very expensive to fabricate on a commercial basis. Thus, general purpose very large scale integration (VLSI) circuits are defined. VLSI circuits serve as many logic roles as possible, which helps to consolidate desired logic functions. However, random logic circuits are still required to tie the various elements of a digital system together.

Several schemes are used to implement these random logic circuits. One solution is standard logic, such as transistor-transistor logic (TTL). TTL integrated circuits are versatile because they integrate only a relatively small number of commonly used logic functions. The drawback is that large numbers of TTL integrated circuits are typically required for a specific application. This increases the consumption of power and board space, and drives up the overall cost of the digital system.

One alternative to standard logic is fully custom logic integrated circuits. Custom logic circuits are precisely tailored to the needs of a specific application. This allows the implementation of specific circuit architectures that dramatically reduces the number of parts required for a system. However, custom logic devices require significantly greater engineering time and effort, which increases the cost to develop these circuits and may also delay the production of the end system.

A less expensive alternative to custom logic is the "programmable logic array." Programmable logic arrays take advantage of the fact that complex combinational logic functions can be reduced and simplified into various standard forms. For example, logical functions can be manipulated and reduced down to traditional Sum of Products (SOP) form. In SOP form, a logical function uses just two types of logic functions that are implemented sequentially. This is referred to as two-level logic and can be implemented with various conventional logic functions, e.g., AND-OR, NAND-NAND, NOR-NOR.

One benefit of the programmable logic array is that it provides a regular, systematic approach to the design of random, combinational logic circuits. A multitude of logical functions can be created from a common building block, e.g., an array of transistors. The logic array is customized or "programmed" by creating a specific metallization pattern to interconnect the various transistors in the array to implement the desired function.

Programmable logic arrays are fabricated using photolithographic techniques that allow semiconductor and other

materials to be manipulated to form integrated circuits as is known in the art. These photolithographic techniques essentially use light that is focused through lenses and masks to define patterns in the materials with microscopic dimensions. The equipment and techniques that are used to implement this photolithography provide a limit for the size of the circuits that can be formed with the materials. Essentially, at some point, the lithography cannot create a fine enough image with sufficient clarity to decrease the size of the elements of the circuit. In other words, there is a minimum dimension that can be achieved through conventional photolithography. This minimum dimension is referred to as the "critical dimension" (CD) or minimum "feature size" (F) of the photolithographic process. The minimum feature size imposes one constraint on the size of the components of a programmable logic array. In order to keep up with the demands for larger programmable logic arrays, designers search for ways to reduce the size of the components of the array.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a programmable logic array that uses less surface area of a semiconductor wafer as compared to conventional arrays.

SUMMARY OF THE INVENTION

The above mentioned problems with programmable logic arrays and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A programmable logic array is described which is formed with vertical transistors.

In one embodiment, a programmable logic array is provided. The programmable logic array includes first and second logic planes. The first logic plane receives a number of input signals. The first logic plane includes a plurality of vertical transistors arranged in rows and columns that are interconnected to provide a number of logical outputs. The second logic plane also includes a number of vertical transistors arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified block diagram of a high-level organization of a digital computer including one or more programmable logic arrays formed with vertical transistors according to the teachings of the present invention.

FIG. 2 is a simplified block diagram of an embodiment of a programmable logic array according to the teachings of the present invention.

FIG. 3 is a schematic diagram of one embodiment of a programmable logic array according to the teachings of the present invention.

FIGS. 4 through 11 are top and front views that illustrate a number of embodiments of a logic plane according to the teachings of the present invention.

FIGS. 12, 13A, 13B, 14, 15, 16, 17, 18, 19, 20, and 21 illustrate generally various stages of one embodiment of a method of forming an array of logic cells according to the teachings of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the invention, reference is made to the accompanying drawings which

form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or the substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on," "side," (as in sidewall), "higher," "lower," "over," and under are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Throughout this specification the designation "n+" refers to semiconductor material that is heavily doped n-type semiconductor material, e.g., monocrystalline silicon or polycrystalline silicon. Similarly, the designation "p+" refers to semiconductor material that is heavily doped p-type semiconductor material. The designations "n-" and "p-" refer to lightly doped n and p-type semiconductor materials, respectively.

FIG. 1 is a simplified block diagram of a high-level organization of a digital computer 10. A digital computer 10 is a system whose functional elements consist of an arithmetic/logic unit (ALUs) 20, a control unit 30, a memory unit 40 and an input/output (I/O) device 50. Every computer system has a native set of instructions that specify operations to be performed on data by the ALU 20 and other interactions between the ALU 20, the memory unit 40 and the I/O devices 50. The memory units 40 contain the data plus a stored list of instructions.

The control unit 30 coordinates all operations of the ALU 20, the memory unit 40 and the I/O devices 50 by continuously cycling through a set of operations that cause instructions to be fetched from the memory unit 40 and executed. Many of the logic functions performed by these components can include a programmable logic array with vertical transistors according to the teachings of the present invention. With respect to the ALU 20, the control unit 30 and the I/O devices 50, arbitrary logic functions may be realized in the "sum-of-products" form. A logic function sum-of-products may be implemented using any of the equivalent two-level logic configurations: AND-OR, NAND-NAND, NOR-OR, OR-NOR, AND-NOR, NAND-AND or OR-AND.

FIG. 2 is a simplified diagram of a programmable logic array (PLA), indicated generally at 100, and constructed according to the teachings of the present invention. PLA 100 includes two major constituents: a first logic plane 120 and a second logic plane 130. The first and second logic planes 120 and 130 are formed using an array of vertical transistors. In one embodiment, the first and second logic planes 120 and 130 each comprise NOR logic circuits such that PLA 100 implements NOR-NOR logic. In other embodiments, first and second logic planes 120 and 130 are constructed from arrays of vertical transistors that are configured to implement AND-OR, OR-AND, NAND-NAND, NOR-OR, OR-NOR, AND-NOR, and NAND-AND logic.

Input lines 125 are coupled to receive a number of input signals. Inverters/drivers 150 are coupled to the input lines 125 such that first logic plane 120 is capable of receiving each of the input signals and their complements. First logic plane 120 produces a number of output signals that are logical combinations of the signals from inverters/drivers 150. The output signals from first logic plane 120 are provided to second logic plane 130 via interconnection lines 122. Second logic plane 130 produces a number of output signals that are logical combinations of the signals from interconnection lines 122.

In addition, various control circuits and signals not detailed herein initiate and synchronize the PLA 100 operation as known to those skilled in the art. The PLA 100 implementation described with respect to FIG. 2 is illustrative only and is not intended to be exclusive or limiting.

FIG. 3 is a schematic diagram illustrating generally an architecture of one embodiment of a programmable logic array (PLA), indicated generally at 300, and constructed according to the teachings of the present invention. PLA 300 implements an illustrative logical function using a two level logic approach. Specifically, PLA 300 includes first and second logic planes 310 and 320. In this example, the logic function is implemented using NOR-NOR logic. First and second logic planes 310 and 320 each include an array of vertical transistors that are configured to implement the logical function of PLA 300.

It is noted that the configuration of FIG. 3 is provided by way of example and not by way of limitation. Specifically, the teachings of the present application are not limited to programmable logic arrays in the NOR-NOR approach. Further, the teachings of the present application are not limited to the specific logical function shown in FIG. 3. Other logical functions can be implemented in a programmable logic array with vertical transistors using any one of the various two level logic approaches.

First logic plane 310 receives a number of input signals at input lines 312. In this example, no inverters are provided for generating complements of the input signals. However, first logic plane 310 can include inverters to produce the complementary signals when needed in a specific application.

First logic plane 310 includes a number of vertical transistors that form an array. The transistors are located at the intersection of input lines 312 and interconnect lines 314. Not all of the transistors are operatively connected in the first logic plane. Rather, the transistors are selectively coupled to the input and interconnection lines so as to implement a desired logic function. Thus, some transistors are left unconnected. This selective interconnection is referred to as "mask programming" since the logical function implemented by the programmable logic array is "programmed" into the array by masking steps that are used in the generation of the conductors that interconnect the transistors in the array.

In this embodiment, each of the interconnect lines **314** acts as a NOR gate for the input lines **312** that are connected to the interconnect lines **314** through the transistors of the array. For example, interconnection line **314a** acts as a NOR gate for the signals on input lines **312b** and **312c**. That is, p-channel pull up transistor **316a** maintains interconnect line **314a** at a high potential unless one or more of the transistors that are coupled to interconnect line **314a** are turned on by a high logic level signal on an input line.

In a similar manner, second logic plane **320** comprises a second array of transistors that are selectively interconnected to provide the second level of the two level logic needed to implement a specific logical function. In this embodiment, the array of transistors is also configured such that the output lines **318** comprise a logical NOR function of the signals from the interconnection lines **314** that are coupled to particular output lines through the vertical transistors of the second logic plane **320**.

FIGS. **4** through **11** illustrate a number of embodiments for implementing a logic plane with vertical transistors for use in a programmable logic array. FIGS. **4** and **5**, **6** and **7**, **8** and **9**, and **10** and **11** are top and side views, respectively, of the various embodiments. For purposes of clarity, only a portion of each logic plane is shown in each Figure.

Generally, the logic planes of the illustrated embodiments include a number of pillars of monocrystalline semiconductor material. These pillars form the basis for the vertical transistors of a logic plane. For example, logic plane **350a** of FIGS. **4** and **5** includes pillars **352a**, **354a**, **356a**, and **358a**. The pillars are separated from adjacent pillars by a number of orthogonal trenches.

Each pillar includes at least three vertically aligned regions extending from a semiconductor substrate or insulator layer. Again, with reference to FIG. **5**, pillar **352a** includes first source/drain region **360a**, body region **362a**, and second source/drain region **364a**. As indicated by the Figures, the body regions are lightly doped, e.g., p- semiconductor material, such that the pillar can provide a fully depleted transistor structure with channels formed along a side surface of the body region between the first and second source/drain regions.

The embodiments illustrated in FIGS. **6** through **11** also include this basic architecture for a programmable logic array: an array of monocrystalline semiconductor pillars separated by orthogonal trenches and each having at least three vertically aligned regions.

In each embodiment, the array of pillars can be “programmed” to implement a particular logic function by the selective formation of conductive lines in the trenches that separate adjacent rows of pillars. The conductive lines can be formed by chemical vapor deposition of, for example, metal or polysilicon as described in more detail below. Trenches separating rows of adjacent pillars can house one or two conductive lines. Further, these conductive lines can either form transistor gates or body contacts. In embodiments supporting body contacts, a particular conductive line can provide an input signal to transistors, e.g., a signal to a gate, in the programmable logic array while other conductive lines provide a body bias (fixed or synchronous with a conductive line in a trench on the opposite side of the pillar) for transistors of the array.

With conductive lines passing on each side of a pillar, gates can be formed on both sides of each pillar. Thus, by selectively forming the conductive lines, a single pillar can implement the function of either one transistor, two transistors or half of a transistor, e.g., one conductive line forms

gates for pillars that are on opposite sides of the trench. The layout of the conductive lines of each embodiment is described in turn below.

FIGS. **4** and **5** illustrate a “split gate” embodiment. In this embodiment, two conductive lines are formed in each trench that separates adjacent rows of pillars. For example, conductive lines **366a** and **368a** are formed in trench **370a**. With this architecture, gates can be formed on two, opposite sides of a pillar. For example, conductive lines **368a** and **372a** form gates on opposite sides of pillar **358a**. This allows pillar **358a** to house two transistors; each with a channel region along one of the sides of pillar **358a**. Alternatively, pillar **358a** can implement a single transistor by coupling conductive lines **368a** and **372a** to the same input signal. When a pillar implements the functionality of two transistors, this provides the advantage of increasing the density of the array. However, when a pillar of this embodiment implements a single transistor this provides redundancy on the input signals provided to the transistor.

FIGS. **6** and **7** illustrate an embodiment of a logic plane **350b** with a single conductive line formed between adjacent rows of pillars. The conductive lines in this embodiment form gates for selected pillars to implement a desired logic function for the logic plane. Conductive lines **366b** and **368b** form gates on either sides of pillar **354b**.

FIGS. **8** and **9** illustrate another embodiment of a logic plane **350c**. In this logic plane, two conductive lines are formed in trenches that separate adjacent rows of pillars. Conductive lines **372c** and **368c** form body contacts for pillars **352c** and **354c**, and **356c** and **358c**, respectively. These conductive lines can provide a synchronous or fixed body bias. Conductive lines **366c** and **374c** are formed so as to provide gates for selected pillars of the logic plane. For example, conductive line **366c** forms a gate for pillar **354c** and conductive line **374c** forms a gate for pillar **358c**.

FIGS. **10** and **11** illustrate another embodiment of a logic plane **350d**. In this logic plane, a single conductive line is formed in each trench that separates adjacent rows of pillars. Conductive lines **368d** and **372d** provide a body contact for pillars **352d** and **354d**, and **356d** and **358d**, respectively. Conductive line **366d** selectively gates the pillars on either side of trench **370d** so as to implement a desired logic function for logic plane **350d**.

FIGS. **12**, **13A**, **13B**, **14**, **15**, **16**, **17**, **18**, **19**, **20**, and **21** illustrate generally one embodiment of a method of forming a logic plane for a programmable logic array according to the teachings of the present invention. In this embodiment, a portion of the logic plane, indicated generally at **400** is formed using bulk silicon processing techniques and is described, by way of example, with respect to a particular technology having a minimum lithographic “feature size,” *F*, which is also sometimes referred to as a “critical dimension” (CD), of 0.4 microns. However, the process steps described below can be scaled accordingly for other minimum feature sizes without departing from the scope of the invention.

In FIG. **12**, a P+ silicon starting material is used for substrate **305**. A first source/drain layer **500**, of approximate thickness of 0.2 microns, is formed at a working surface of substrate **305**. In one embodiment, first source/drain layer **500** is N+ silicon formed by ion-implantation of donor dopants into substrate **305**. In another embodiment, first source/drain layer **500** is N+ silicon formed by epitaxial growth of silicon upon substrate **305**. On the first source/drain layer **500**, a semiconductor epitaxial layer **505**, such as P- silicon of 0.4 micron approximate thickness, is formed, such as by epitaxial growth. Layer **505** is referred to as body layer **505**.

A second source/drain layer **510**, such as N+ silicon of 0.1 to 0.2 microns approximate thickness, is formed at a surface of the epitaxial layer **505**, such as by ion-implantation of donor dopants into P- epitaxial layer **505** or by epitaxial growth of N+ silicon on P- epitaxial layer **505**. A thin layer of silicon dioxide (SiO₂), referred to as pad oxide **515**, is deposited on the second source/drain layer **510**. Pad oxide **515** has a thickness of approximately 10 nanometers. A layer of silicon nitride (Si₃N₄), referred to as pad nitride **520**, is deposited on pad oxide **515**. Pad nitride **520** has a thickness of approximately 100 nanometers.

A photoresist layer is deposited outwardly from pad nitride **520**. The photoresist layer is exposed through a mask to define parallel minimum dimension stripes in the Y-direction. In the embodiment of FIG. **13A**, trenches **402** are formed through the stripe pattern in the photoresist layer. Trenches **402** extend through pad nitride **520**, second source/drain layer **510**, body layer **505** and into first source/drain layer **500**. In this case, first source/drain layer **500** is maintained at ground potential to act as a ground plane for logic plane **400**. In the embodiment of FIG. **13B**, trenches **402b** extend through pad nitride **520**, second source/drain layer **510**, body layer **505**, first source/drain layer **500** and into substrate **305**. In this embodiment, the ground plane is divided into a number of separate ground lines for the logic plane.

The remaining steps are described in terms of the embodiment of FIG. **13A** although similar steps can be applied to complete the embodiment of FIG. **13B**. The photoresist is removed by conventional photoresist stripping techniques.

Next, a second set of trenches is formed so as to create an array of semiconductor pillars. Existing trenches **402** are filled with an insulator by, for example, chemical vapor deposition of oxide layer **404**. Oxide layer **404** is planarized with nitride pad **520** such as by chemical mechanical polishing (CMP) or other suitable planarization technique. Another photoresist layer is deposited and masked to define a second set of minimum dimension stripes that are orthogonal to trenches **402**, i.e., in the X-direction. A nitride etchant is used to etch through pad **520**. Next, a selective silicon etchant is used to etch exposed silicon to a depth approximately equal to trenches **402**. A top view of this portion of decoder **400** is shown in FIG. **14**.

With the photoresist layer still in place, exposed portions of oxide layer **404** are removed stopping on the silicon material at the bottom of trenches **402**. The photoresist layer is then removed by conventional photoresist stripping techniques. This leaves the structure as shown in FIG. **15** with trenches **406** separating rows of semiconductor pillars. FIG. **15** explicitly shows pillars **408**, **410**, **412** and **414**. However, it is understood that logic plane **400** includes a large number of pillars that are formed in a number of rows and columns defined by trenches **402** and **406**.

Next, conductive lines and gates are selectively formed in trenches **406**. The gates are formed adjacent to selected pillars such that logic plane **400** implements a desired function. Nitride (Si₃N₄) is deposited by, for example, chemical vapor deposition with a thickness on the order of 10 nanometers. The nitride layer is directionally etched to leave on vertical walls only of trench **406**. Thermal oxide layer **416** is grown on the bottom of trenches **406** to a thickness of approximately 100 nanometers and the nitride layer is stripped from the vertical sidewalls.

Protective oxide layer **418** is formed, for example, by growing a thin thermal oxide layer of approximately 10 nanometers on the side walls of trenches **406**. Intrinsic

polysilicon layer **420** is deposited by, for example, chemical vapor deposition with a thickness of approximately 50 nanometers. Layer **420** is etched by, for example, reactive ion etching (RIE) techniques to leave layer **420** on vertical sidewalls only. This structure is shown in FIG. **16**.

Next, logic plane **400** is mask programmed by selectively removing portions of polysilicon layer **420** adjacent to pillars where a transistor is needed to implement a desired logic function. A gate is then formed adjacent to these pillars. As for the remaining pillars, polysilicon layer **420** acts as a spacer that prevents an address line or inverse address line from being formed sufficiently close to the pillar so as to form a gate of a transistor.

A photoresist layer is applied and selectively exposed through a mask to uncover the sidewalls, and adjacent layer **420**, of selected pillars to implement the desired logical function. The exposed portions of layer **420** are etched from the vertical sidewalls in trenches **406**. The resist is removed and gate insulator **422**, e.g., silicon dioxide, is grown or deposited on the exposed vertical sidewalls. N+ polysilicon is deposited by chemical vapor deposition with a thickness of approximately 50 nanometers. The polysilicon layer is directionally etched to leave layer **424** on vertical surfaces only and to expose the tops of layer **420** as shown in FIG. **17**.

At this point, the process can take one of two paths depending on whether the embodiment incorporates body contacts. If no body contacts are included, all remaining nitride is selectively stripped. Techniques known in the art are used to remove the remaining portions of layer **420** selectively to doped silicon. Oxide is deposited by chemical vapor deposition to fill the recesses in logic plane **400** and to cover the semiconductor pillars. Contacts and wiring are formed using conventional processing techniques to connect columns of pillars.

In the described embodiment, split address lines are shown. It is understood that once the gate oxide is in place, the trench can be filled with N+ polysilicon to create a single address line between the rows of pillars in a non-split address line embodiment.

If body contacts are included in the embodiment, the process proceeds with the formation of these contacts as shown in FIGS. **18** through **21**.

Nitride layer **430** is deposited using, for example, chemical vapor deposition to a level approximately 20 nanometers above nitride pads **520**. Photoresist layer **432** is deposited and exposed through a mask to form a stripe pattern in the X-direction. Nitride layer **430** is etched briefly to expose alternate polysilicon layers **424** located in the openings of photoresist layer **432** as shown in FIG. **18**.

Exposed polysilicon layers **424** are removed using an etching technique and photoresist layer **432** is removed. An oxide material is deposited in the space vacated by the polysilicon. The oxide material is planarized to the level of nitride layer **430**. The oxide material is directionally etched with a reactive ion etch sufficiently to expose P- layer **505** of the pillars leaving oxide layer **434** at the bottom of trenches **406** as shown in FIG. **19**.

P+ polysilicon **436** is deposited on layer **434** using chemical vapor deposition and planarized with nitride layer **430**. The P+ polysilicon is etched back to below the junction of layers **510** and **505** to form body contacts as shown in FIGS. **20** and **21**.

CONCLUSION

Embodiments of the present invention provide a programmable logic array with an increased density with respect to

conventional arrays. Specifically, vertical transistors are used with conductive lines formed in trenches that separate adjacent rows of semiconductor pillars. The vertical transistors are selectively coupled by mask programming to form these lines so as to implement a desired logical function. It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. For example, the logical function implemented by the programmable logic array can be varied without departing from the scope of the present invention. Further, the size of the array, the number of inputs, the number of interconnects, and the number of outputs can similarly be varied.

What is claimed is:

1. A programmable logic array, comprising:
 - a first logic plane that receives a number of input signals, the first logic plane having a plurality of vertical transistors, each having a first source/drain region, a body region and a second source/drain region, wherein the vertical transistors include one gate that is formed in a trench adjacent to the body region and have a body contact that is formed adjacent to the body region on a side opposite the gate, wherein the body contact is pulsed in synchronization with the gate, and wherein the vertical transistors are arranged in rows and columns that are interconnected to provide a number of logical outputs; and
 - a second logic plane having a number of vertical transistors arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function.
2. The programmable logic array of claim 1, wherein the first logic plane and the second logic plane each comprise NOR planes.
3. The programmable logic array of claim 1, wherein the vertical transistors each comprise a first source/drain region, a body region and a second source/drain region that are vertically aligned in a monocrystalline semiconductor pillar and that extend outwardly from a semiconductor substrate.
4. The programmable logic array of claim 3, wherein the vertical transistors in the second logic plane include one gate that is formed in a trench adjacent to the body region.
5. The programmable logic array of claim 3, wherein the vertical transistors in the second logic plane include one gate that is formed in a trench adjacent to the body region and a body contact that is formed adjacent to the body region on a side opposite the gate.
6. The programmable logic array of claim 3, wherein the vertical transistors include first and second gates that are formed in trenches adjacent to the body region on opposite sides of the pillar.
7. The programmable logic array of claim 3, wherein the trench separates adjacent rows of pillars and the trench houses one input line that is coupled to gates of selected transistors on either side of the trench.
8. The programmable logic array of claim 3, wherein the trench separates adjacent rows of pillars and the trench houses two input lines that are each coupled to gates of selected transistors on one side of the trench.
9. The programmable logic array of claim 3, wherein the trench separates adjacent rows of pillars and the trench houses an input line that is coupled to gates of selected transistors on one side of the trench and a body contact line that is coupled to the body region of each pillar on the other side of the trench.

10. The programmable logic array of claim 1, wherein the substrate is a bulk semiconductor.

11. The programmable logic array of claim 1, wherein the working surface of the substrate includes an insulating layer formed on top of an underlying semiconductor.

12. The programmable logic array of claim 1, wherein the programmable logic array is operatively coupled to a computer system.

13. The programmable logic array of claim 5, wherein the body contact is maintained at a substantially constant voltage.

14. The programmable logic array of claim 5, wherein the body contact in the second logic plane is pulsed in synchronization with the gate.

15. The programmable logic array of claim 3, wherein the body region comprises a lightly doped body region such that the transistor functions as a fully depleted transistor.

16. The programmable logic array of claim 3, wherein the first source/drain regions of the pillars of the array are coupled together.

17. A computer system, comprising:

- at least one input/output device;
- a memory; and
- a central processing unit, the central processing unit coupled to the memory and the at least one input/output device, the central processing unit including at least one programmable logic array including:
 - a first logic plane that receives a number of input signals, the first logic plane having a plurality of vertical transistors, each having a first source/drain region, a body region and a second source/drain region, wherein the vertical transistors include one gate that is formed in a trench adjacent to the body region and have a body contact that is formed adjacent to the body region on a side opposite the gate, wherein the body contact is pulsed in synchronization with the gate, and wherein the vertical transistors are arranged in rows and columns that are interconnected to provide a number of logical outputs; and
 - a second logic plane having a number of vertical transistors arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function for the central processing unit.
- 18. The computer system of claim 17, wherein the first logic plane and the second logic plane each comprise NOR planes.
- 19. The computer system of claim 17, wherein the vertical transistors in the second logic plane each comprise a first source/drain region, a body region and a second source/drain region that are vertically aligned in a monocrystalline semiconductor pillar and that extend outwardly from a semiconductor substrate.
- 20. The computer system of claim 19, wherein the vertical transistors in the second logic plane include one gate that is formed in a trench adjacent to the body region.
- 21. The computer system of claim 19, wherein the vertical transistors in the second logic plane include one gate that is formed in a trench adjacent to the body region and a body contact that is formed adjacent to the body region on a side opposite the gate.
- 22. The computer system of claim 19, wherein the vertical transistors include first and second gates that are formed in trenches adjacent to the body region on opposite sides of the pillar.

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23. The computer system of claim **19**, wherein the trench separates adjacent rows of pillars and the trench houses one input line that is coupled to gates of selected transistors on either side of the trench.

24. The computer system of claim **19**, wherein the trench separates adjacent rows of pillars and the trench houses two input lines that are each coupled to gates of selected transistors on one side of the trench.

25. The computer system of claim **19**, wherein the trench separates adjacent rows of pillars and the trench houses an input line that is coupled to gates of selected transistors on one side of the trench and a body contact line that is coupled to the body region of each pillar on the other side of the trench.

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26. The computer system of claim **17**, wherein the substrate is a bulk semiconductor.

27. The computer system of claim **17**, wherein the working surface of the substrate includes an insulating layer formed on top of an underlying semiconductor.

28. The computer system of claim **21**, wherein the body contact is maintained at a substantially constant voltage.

29. The computer system of claim **19**, wherein the body region comprises a lightly doped body region such that the transistor functions as a fully depleted transistor.

30. The computer system of claim **19**, wherein the first source/drain regions of the pillars of the array are coupled together.

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