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(54) **STRUCTURE AND METHOD FOR A HIGH PERFORMANCE ELECTRONIC PACKAGING ASSEMBLY**

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(52) **U.S. Cl.** **438/108**; 438/612; 438/655; 257/723

(58) **Field of Search** 257/686, 689, 257/690, 777, 778, 779, 780, 782, 783; 438/106, 107, 108, 109, 110, 612, 655

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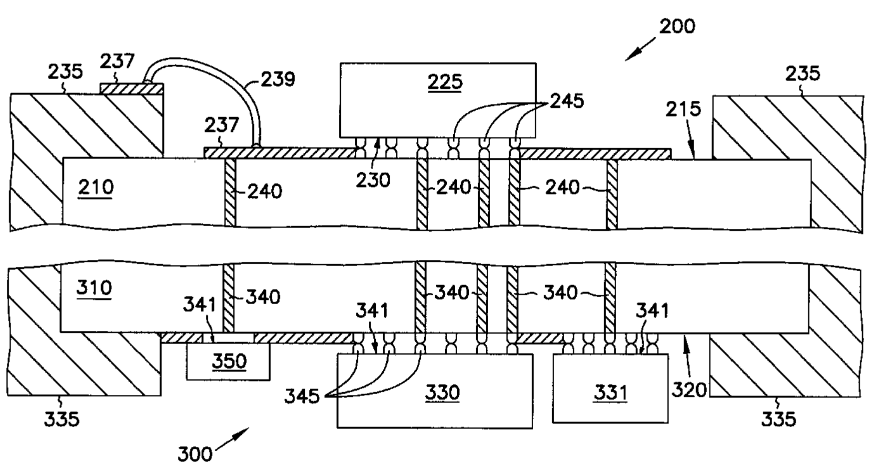
(57) **ABSTRACT**

An improved structure and method are provided for increasing the operational bandwidth between different circuit devices, e.g. logic and memory chips, without requiring changes in current CMOS processing techniques. The structure includes the use of a silicon interposer. The silicon interposer can consist of recycled rejected wafers from the front-end semiconductor processing. Micro-machined vias are formed through the silicon interposer. The micro-machined vias include electrical contacts which couple various integrated circuit devices located on the opposing surfaces of the silicon interposer.

27 Claims, 3 Drawing Sheets



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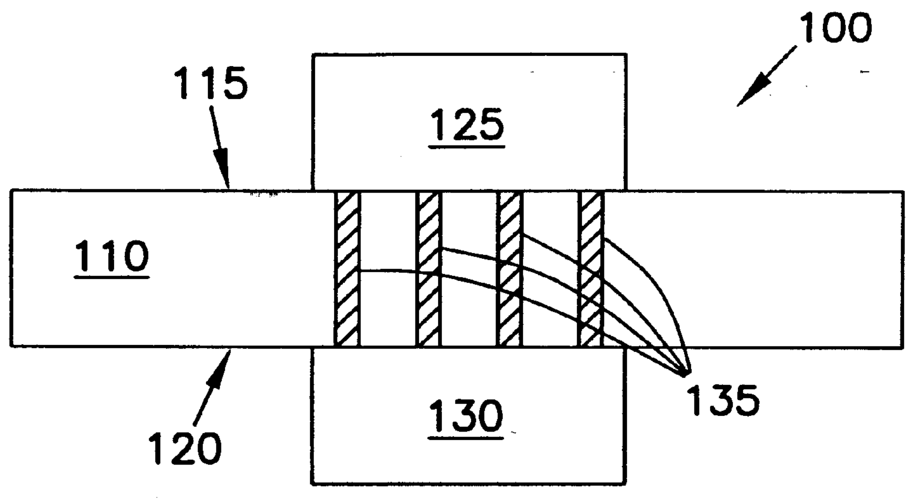
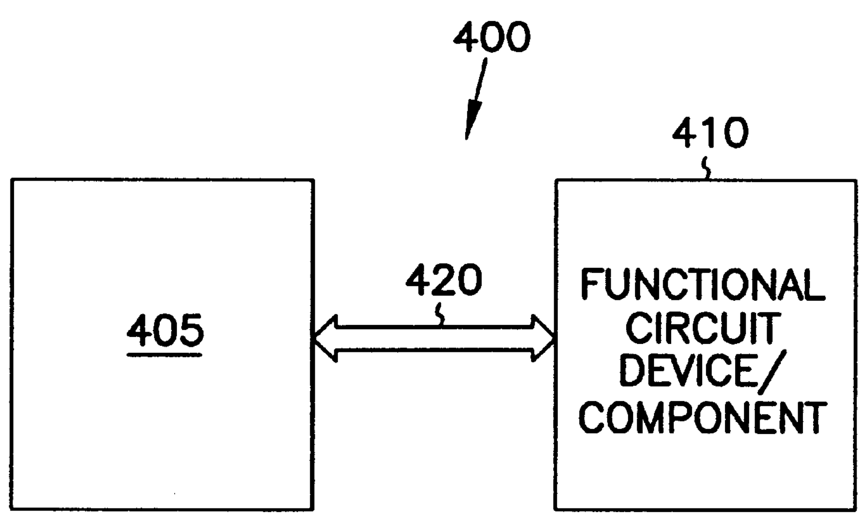


100
115
125
110
135
130
120

FIG. 1



400
410
405
420
FUNCTIONAL CIRCUIT DEVICE/ COMPONENT

FIG. 4

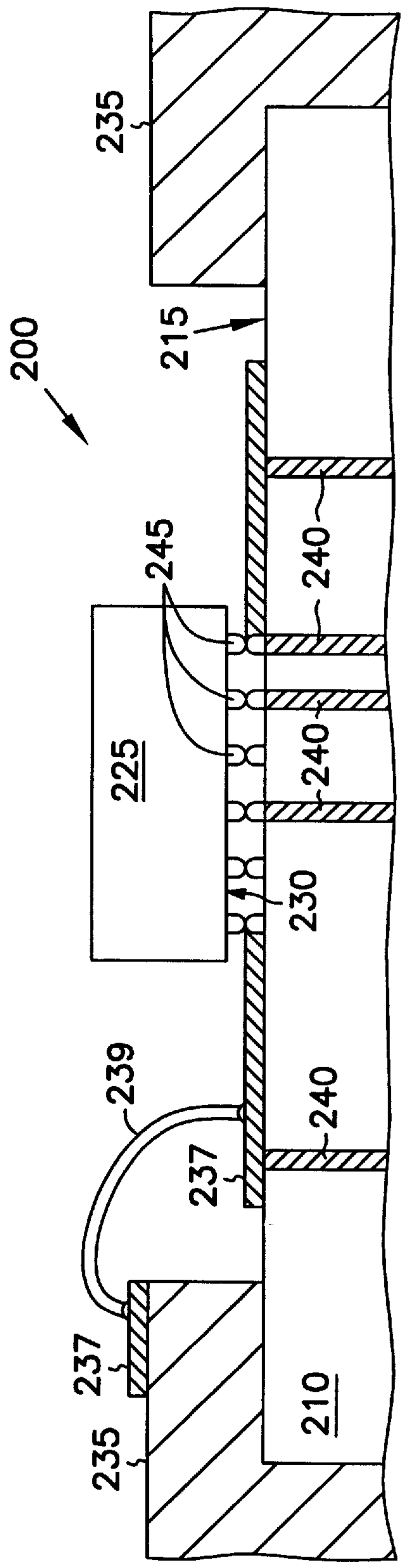

200
235
215
245
225
240
240
240
230
239
240
237
237
235
210

FIG. 2

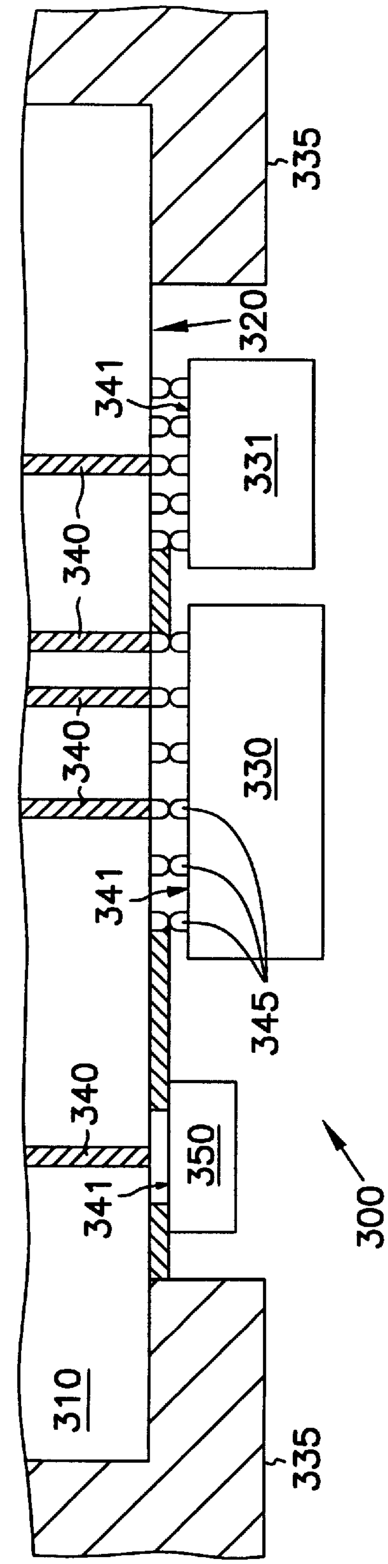

335
320
341
331
340
340
330
340
341
345
340
350
341
300
310
335

FIG. 3

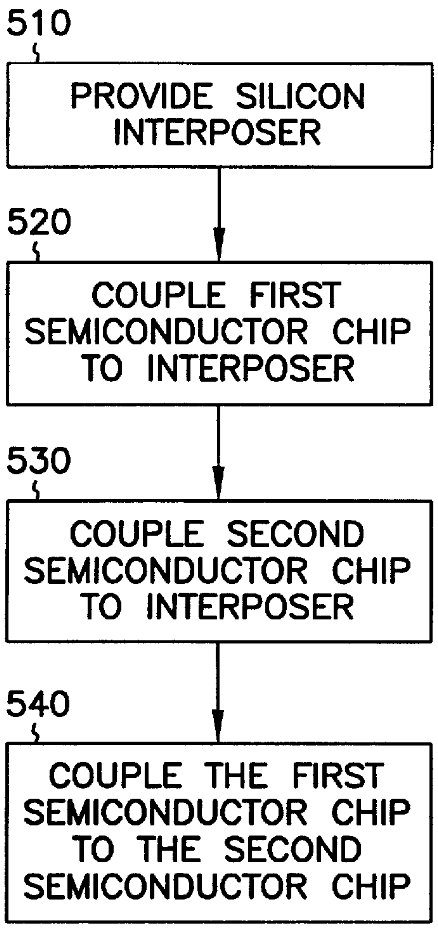

510
PROVIDE SILICON INTERPOSER
520
COUPLE FIRST SEMICONDUCTOR CHIP TO INTERPOSER
530
COUPLE SECOND SEMICONDUCTOR CHIP TO INTERPOSER
540
COUPLE THE FIRST SEMICONDUCTOR CHIP TO THE SECOND SEMICONDUCTOR CHIP

FIG. 5

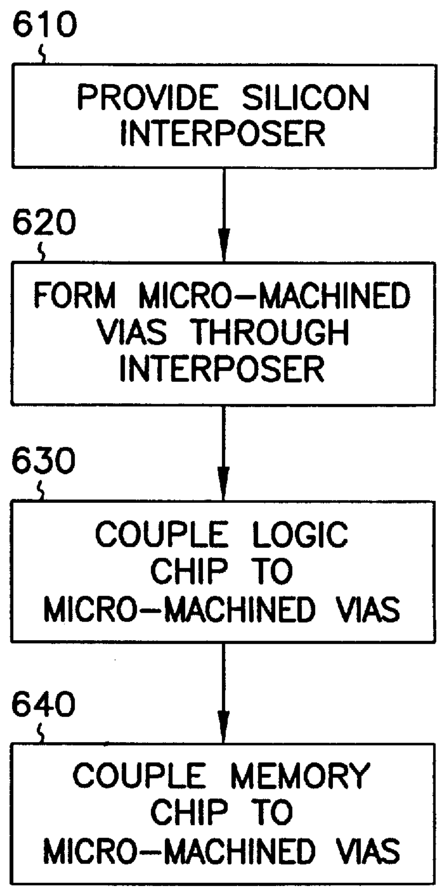

610
PROVIDE SILICON INTERPOSER
620
FORM MICRO-MACHINED VIAS THROUGH INTERPOSER
630
COUPLE LOGIC CHIP TO MICRO-MACHINED VIAS
640
COUPLE MEMORY CHIP TO MICRO-MACHINED VIAS

FIG. 6

STRUCTURE AND METHOD FOR A HIGH PERFORMANCE ELECTRONIC PACKAGING ASSEMBLY

FIELD OF THE INVENTION

The present invention relates generally to semiconductor integrated circuits. More particularly, it pertains to a structure and method for a high performance electronic packaging assembly.

BACKGROUND OF THE INVENTION

Integrated circuit technology relies on transistors to formulate vast arrays of functional circuits. The complexity of these circuits requires the use of an ever increasing number of linked transistors. As the number of transistors required increases, the integrated circuitry dimensions shrink. One challenge in the semiconductor industry is to develop improved methods for electrically connecting and packaging circuit devices which are fabricated on the same and on different wafers or chips. It is an objective in the semiconductor industry to construct transistors which occupy less surface area on the silicon chip/die.

As integrated circuit technology progresses there is a growing desire for a "system on a chip." Ideally, a computing system would be fabricated with all the necessary integrated circuits on one wafer, as compared with today's method of fabricating many chips of different functions and packaging them to assemble. a complete system. Such a structure would greatly improve integrated circuit performance and provide higher bandwidth. In practice, it is very difficult with today's technology to implement a truly high-performance "system on a chip" because of vastly different fabrication processes and different manufacturing yields for the logic and memory circuits. Thus, what is needed is an improved method and structure which continues to approach the ideal set-up of a "system on a chip" and thus improves the integration of different chips in an integrated circuit.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, it is desirable to develop a structure and method to increase the operational speeds, or data bandwidth, between different circuit devices, e.g. logic and memory chips. It is further desirable to attain this ability using current CMOS fabrication techniques.

SUMMARY OF THE INVENTION

The above mentioned problems with integrated circuits and other problems are addressed by the present invention and will be understood by reading and studying the following specification. A structure and method are provided to maximize the bandwith between different circuit devices.

In particular, an illustrative embodiment of the present invention includes an electronic packaging assembly. The electronic packaging assembly includes a silicon interposer which has a first and second side. At least one semiconductor chip is located on a first side of the silicon interposer. At least one semiconductor chip is located on a second side of the silicon interposer. A number of electrical connections exist through the silicon interposer which couple the semiconductor chips located on each side of the silicon interposer.

In another embodiment, an electronic system module is provided. The electronic system module includes a silicon interposer which has opposing surfaces. A microprocessor is included which has a circuit side. The circuit side of the microprocessor faces a first one of the opposing surfaces of the silicon interposer. A first memory chip is included which has a circuit side. The circuit side of the memory chip faces a second one of the opposing surfaces of the silicon interposer. Further, a number of electrical connections are provided which extend through the silicon interposer. The number of electrical connections couple the circuit side of the microprocessor to the circuit side of the first memory chip.

In another embodiment, a computer system is provided. The computer system includes an electronic packaging assembly. The electronic packaging assembly includes the electronic packaging assembly presented and described above. A number of external devices are included. A system bus couples the electronic packaging assembly to the number of external devices.

In another embodiment, a method for forming integrated circuits is provided. The method includes providing a silicon interposer which has opposing sides. A first semiconductor chip is coupled to a first side of the silicon interposer. A second semiconductor chip is coupled to a second side of the silicon interposer. The method further includes coupling the first semiconductor chip to the second semiconductor chip by means of electrical connections through the silicon interposer.

In an alternative embodiment, a method for forming integrated circuit is provided. The method includes providing a silicon interposer which has opposing sides. A number of micro-machined vias are formed through the silicon interposer. The micro-machined vias include a number of electrical connections between the opposing surfaces of the silicon interposer. A logic chip is coupled to the number of micro-machined vias on a first side of the silicon interposer. The method further includes coupling a memory chip to the number of micro-machined vias on a second side of the silicon interposer.

Thus, an improved structure and method are provided. The structure and method increase the operational bandwidth between different circuit devices, e.g. logic and memory chips, without requiring changes in current CMOS processing techniques. The structure includes the use of a silicon interposer. The silicon interposer can consist of recycled rejected wafers from the front-end semiconductor processing. This provides the added advantage of low cost and availability. A silicon interposer is thermally matched to the circuit devices such that coefficient of expansion mismatches are nonexistent. And, deposition of conductors on the silicon interposer's surface is readily accomplished using a standard integrated circuit multi-layer metallurgy.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view illustrating an electronic packaging assembly according to the teachings of the present invention.

FIG. **2** is a cross-sectional view illustrating in greater detail a portion of a first one of opposing surfaces for the electronic packaging assembly of FIG. **1**.

FIG. **3** is a cross-sectional view illustrating in greater detail a portion of a second one of opposing surfaces for the electronic packaging assembly of FIG. **1**.

FIG. **4** is a block diagram illustrating a computer system according to an embodiment of the present invention.

FIG. **5** illustrates, in flow diagram form, a methodical aspect according to the teachings of the present invention.

FIG. **6** illustrates, in flow diagram form, another methodical aspect according to the teachings of the present invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizonal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Throughout this specification the designation "n+" refers to semiconductor material that is heavily doped n-type semiconductor material, e.g., monocrystalline silicon or polycrystalline silicon. Similarly, the designation "p+" refers to semiconductor material that is heavily doped p-type semiconductor material. The designations "n−" and "p−" refer to lightly doped n and p-type semiconductor materials, respectively.

FIG. **1** is a cross-sectional view illustrating an electronic packaging assembly **100** according to the teachings of the present invention. According to an alternative embodiment, the electronic packaging assembly **100** can be implemented as an electronic system module. FIG. **1** includes a silicon interposer **110**. The silicon interposer **110** has opposing surfaces which include a first one **115** of the opposing surfaces, or first side **115** and a second one **120** of opposing surfaces, or second side **120**. In one exemplary embodiment, the silicon interposer **110** includes rejected silicon wafers which have been recycled from the front-end of the semiconductor fabrication process. The assembly **100** includes at least one semiconductor chip **125** on the first side **115** of the silicon interposer **110**. In one exemplary embodiment, the at least one semiconductor chip **125** on the first side **115** includes a microprocessor chip. In another embodiment, the at least one semiconductor chip **125** includes any suitable logic chip.

The electronic packaging assembly of FIG. **1** further illustrates at least one semiconductor chip **130** on the second side **120** of the silicon interposer **110**. In one exemplary embodiment, the at least one semiconductor chip **130** on the second side **120** of the silicon interposer includes a memory chip. The memory chip can include a dynamic random access memory (DRAM)-type chip. Likewise, the memory chip can include a static random access memory (SRAM)-type chip or flash electrically erasable program read only memory (flash EEPROM) type chip.

FIG. **1** illustrates that the at least one semiconductor chip **125** located on the first side **115** of the silicon interposer **110** is coupled to the at least one semiconductor chip **130** located on the second side **120** of the silicon interposer **110** by a number of electrical connections **135**. The number of electrical connections **135** include micro-machined vias. The number of electrical connections **135** may be formed using, for example, the techniques shown and described with respect to FIGS. **1–8** of co-pending application Ser. No. 08/917,443, entitled "Integrated Circuitry and Methods of Forming Integrated Circuitry," filed on Aug. 22, 1997 or with respect to FIGS. **1–13** of application Ser. No. 08/917,449, entitled "Methods of Forming Coaxial Integrated Circuitry Interconnect Lines, and Integrated Circuitry," filed on Aug. 22, 1997, which applications are incorporated herein by reference.

FIG. **2** is a cross-sectional view illustrating in greater detail a portion of an embodiment of an electronic packaging assembly **200**. The electronic packaging assembly **200** includes a silicon interposer **210**. FIG. **2** illustrates a first one **215** of opposing surfaces of the silicon interposer **210**. At least one semiconductor chip **225** is coupled to the first one **215** of opposing sides of the silicqn interposer **210**. FIG. **2** additionally illustrates illustrates that the silicon interposer **210** includes a number of electrical connections **240** which extend through the silicon interposer **210**.

The number of electrical connections **240** include micro-machined vias **240**. In one embodiment, the number of electrical connections **240** include micropores which penetrate the silicon interposer **210** and are formed from deposited dielectrics and conductors to form coaxial wiring. In this embodiment, the number of electrical connections **240** may be formed using, for example, the techniques shown or described with respect to FIGS. **1–13** of application Ser. No. 08/917,449, entitled "Methods of Forming Coaxial Integrated Circuitry Interconnect Lines, and Integrated Circuitry," filed on Aug. 22, 1997, which application is incorporated herein by reference. In an alternative embodiment, the number of electrical connections **240** includes salicided connections. In this embodiment, the number of electrical connections **240** may be formed using, for example, the techniques shown and described with respect to FIGS. **1–8** of co-pending application Ser. No. 08/917,443, entitled "Integrated Circuitry and Methods of Forming Integrated Circuitry," filed on Aug. 22, 1997, which application is incorporated by reference.

In one exemplary embodiment, the at least one semiconductor chip **225** includes a microprocessor chip **225**. In another embodiment, the at least one semiconductor chip **225** includes any suitable logic chip **225**. The microprocessor chip **225** has a circuit side **230**. The circuit side **230** of the microprocessor chip **225** faces the first one **215** of the opposing surfaces of the silicon interposer **210**. Electrical contacts **245** couple the circuit side **230** of the microprocessor chip **225** to the number of electrical connections **240**. In one embodiment, a ball grid array (BGA) **245** couples the circuit side **230** of the microprocessor chip **225** to the number of electrical connections **240**. Each ball grid array is encapsulated for passivation and to eliminate electrical contact failures caused by vibration, shock, and thermal cycling. In an alternate embodiment, the circuit side **230** is coupled to the number of electrical connections **240** by any suitable electrical contact **245**.

FIG. **2** illustrates that the silicon interposer **210** is further connected to an integrated circuit package **235**, or chip package **235**. One of ordinary skill in the art of semiconductor fabrication will understand the manner by which the silicon interposer **210** may be connected to the chip package **235**. The chip package **235** and the silicon interposer have electrical lead pads **237**, or metal connects, **237**. FIG. **2** illustrates that the electronic packaging assembly **200** includes electrical coupling **239** between the chip package **235** and the silicon interposer **210**. In one embodiment, the electrical coupling **239** includes wire bonding. In an alternative embodiment, the electrical coupling **239** includes any suitable coupling as the same is known and practiced by those of ordinary skill in the field of semiconductor fabrication. Also, according to this structural arrangement, the back side of the microprocessor chip **225** is exposed to cooling air. The back side of the microprocessor chip **225** can, alternatively or additionally, be contacted bya suitable heat sink to provide heat removal.

FIG. **3** is a cross-sectional view illustrating in greater detail a portion of an embodiment of an electronic packaging assembly **300**. The electronic packaging assembly **300** includes a silicon interposer **310**. In FIG. **3**, a number of electrical connections **340** extend through the silicon interposer **310**. The number of electrical connections **340** include micro-machined vias. In one embodiment, the number of electrical connections **340** include micropores which penetrate the silicon interposer **310** and are formed from deposited dielectrics and conductors to form coaxial wiring. In this embodiment, the number of electrical connections **340** may be formed using, for example, the techniques shown or described with respect to FIGS. **1–13** of application Ser. No. 08/917,449, entitled "Methods of Forming Coaxial Integrated Circuitry Interconnect Lines, and Integrated Circuitry," filed on Aug. 22, 1997, which application is incorporated herein by reference. In an alternative embodiment, the number of electrical connections **340** includes salicided connections. In this embodiment, the number of electrical connections **340** may be formed using, for example, the techniques shown and described with respect to FIGS. **1–8** of copending application Ser. No. 08/917,443, entitled "Integrated Circuitry and Methods of Forming Integrated Circuitry," filed on Aug. 22, 1997, which application is incorporated by reference.

In FIG. **3**, a second one **320** of opposing surfaces of the silicon interposer **310** is shown. At least one semiconductor chip **330** is coupled to the second side **320** of the silicon interposer **310**. In one exemplary embodiment, the at least one semiconductor chip **330** on the second side **320** of the silicon interposer **310** includes a memory chip **330**. The memory chip **330** can include a dynamic random access memory (DRAM)-tape chip. Likewise, the memory chip **330** can include a static random access memory (SRAM)-tape chip or a flash EEPROM type chip.

FIG. **3** illustrates that the electronic packaging assembly **300** can include a second semiconductor chip **331** on the second side **320** of the silicon interposer **310**. In one exemplary embodiment, the second semiconductor chip **331** includes a second memory chip **331**. Like before, the second memory chip **331** can include a dynamic random access memory (DRAM)type chip. And, the second memory chip **331** can include a static random access memory (SRAM)-type chip or a flash EEPROM type chip. FIG. **3** additionally illustrates that the electronic packaging assembly **300** can include a capacitor **350** on the second side **320** of the silicon interposer **310**.

The memory chip **330**, the second memory chip **331**, and the capacitor **350** each have a circuit side **341**. The circuit side **341** of each faces the second one **320** of the opposing surfaces of the silicon interposer **310**. Electrical contacts **345** couple each circuit side **341** of the memory chip **330**, the second memory chip **331**, and the capacitor **350** to the number of electrical connections **340**. In one embodiment, a ball grid array (BGA) **345** is used to couple each circuit side **341** of the memory chip **330**, the second memory chip **331**, and the capacitor the number of electrical connections **340**. Each ball grid array is encapsulated for passivation and to eliminate electrical contact failures caused by vibration, shock, and thermal cycling. In an alternate embodiment, each circuit side **341** is coupled to the number of electrical connections **340** by any suitable electrical contact **345**.

As shown in FIG. **3**, silicon interposer **310** is connected to a chip package **335**. One of ordinary skill in the art of semiconductor fabrication will understand the manner by which the silicon interposer **310** may be connected to the chip package **335**.

FIG. **4** is a block diagram illustrating a computer system **400** according to an embodiment of the present invention. The computer system **400** includes an electronic packaging system **405**. The electronic packaging system **405** includes the electronic packaging system **465** presented and described in detail above. The computer system **400** includes a number of external devices **410**. The number of external devices **410** include, for example, memory controllers, microprocessors and input/output bus units. The computer system **400** includes a system bus **420**. The system bus **420** couples the number of eiternal devices **410** to the electronic packaging system **405**.

FIG. **5** illustrates, in flow diagram form, a methodical aspect according to the teachings of the present invention. A silicon interposer is provided at **510**. A first semiconductor chip is coupled to the silicon interposer at **520**. Next, a second semiconductor chip is coupled to the silicon interposer at **530**. The first and second semiconductor chips are coupled to each other at **540**, preferably in a manner described above.

FIG. **6** illustrates, in flow diagram form, another methodical aspect according to the teachings of the present invention. A silicon interposer is provided at **610**. Micro-machined vias are formed through the silicon interposer at **620**, preferably in a manner described above. A first semiconductor chip is coupled to the micro-machined vias at **620**. And, a second semiconductor chip is coupled to the micro-machined vias at **640**.

CONCLUSION

An improved structure and method for integrating different chips in a integrated circuit is provided. The structure and method increase the operational bandwidth between different circuit devices, e.g. logic and memory chips, without requiring changes in current CMOS processing techniques. The structure includes the use of a silicon interposer. The silicon interposer can consist of recycled rejected wafers from the front-end semiconductor processing. This provides the added advantage of low cost and availability. A silicon interposer is thermally matched to the package circuits components such that coefficient of expansion mismatches are nonexistent And, deposition of conductors on the silicon interposer's surface is readily accomplished using a standard integrated circuit multi-layer metallurgy.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method for forming integrated circuits, comprising:

providing a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer; and

coupling the first semiconductor chip to the second semiconductor chip by forming a number of micro-machined vias to create electrical connections through the silicon interposer.

2. The method of claim **1**, wherein providing the silicon interposer having opposing sides includes providing a silicon interposer formed from recycled silicon wafers.

3. The method of claim **1**, wherein coupling the first semiconductor chip to the first side of the silicon interposer includes coupling a microprocessor chip to the first side.

4. The method of claim **1**, wherein coupling the second semiconductor chip to the second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

5. The method of claim **1**, further including coupling a capacitor to the second side of the silicon interposer.

6. A method for forming integrated circuits, comprising:

providing a silicon interposer having opposing sides;

forming a number of micro-machined vias through the silicon interposer, wherein the micro-machined vias include a number of electrical connections between the opposing surfaces of the silicon interposer;

coupling a logic chip to the number of micro-machined vias on a first side of the silicon interposer; and

coupling a memory chip to the number of micro-machined vias on a second side of the silicon interposer.

7. The method of claims **6**, wherein coupling the memory chip includes coupling a DRAM chip.

8. The method of claim **6**, wherein coupling the memory chip includes coupling a SRAM chip.

9. The method of claims **6**, wherein coupling the memory chip includes coupling a flash EEPROM chip.

10. The method of claim **6**, wherein coupling the logic and memory chips to the number of micro-machined vias includes using a ball grid array.

11. The method of claim **6**, further including cooling the logic chip on the first side of the silicon interposer.

12. The method of claim **6**, wherein coupling the logic chip to the first side of the silicon interposer includes coupling the logic chip to an integrated circuit package.

13. The method of claims **12**, wherein coupling the logic chip to the integrated circuit package includes bonding the logic chip to the integrated circuit package.

14. A method for forming an electronic packaging assembly, comprising:

forming a number of micro-machined vias through a silicon interposer having opposing sides;

coupling a first semiconductor chip to a first side of the silicon interposer;

coupling a second semiconductor chip to a second side of the silicon interposer; and

electrically coupling the first semiconductor chip to the second semiconductor chip using the number of micro-machined vias.

15. The method of claim **14**, wherein forming the number of micro-machined vias through the silicon interposer includes forming salicided connections in the number of micro-machined vias.

16. A method for forming an electronic system module, comprising:

forming a number of micro-machined vias through a silicon interposer having opposing sides;

coupling at least one semiconductor chip to a first side of the silicon interposer;

coupling at least one semiconductor chip to a second side of the silicon interposer; and

electrically coupling the at least one semiconductor chip on the first side of the silicon interposer to the at least one semiconductor chip on the second side of the silicon interposer using the number of micro-machined vias.

17. The method of claim **16**, wherein forming a number of micro-machined vias through a silicon interposer having opposing sides includes forming the number of micro-machined vias through a silicon interposer formed from recycled silicon wafers.

18. The method of claim **16**, wherein coupling at least one semiconductor chip to a first side of the silicon interposer includes coupling a microprocessor chip to the first side.

19. The method of claim **16**, wherein coupling at least one semiconductor chip to a second side of the silicon interposer includes coupling a memory chip to the second side of the silicon interposer.

20. The method of claim **16**, wherein the method further includes coupling a capacitor to the second side of the silicon interposer.

21. A method for forming an electronic system module, comprising:

forming a number of micro-machined vias through a silicon interposer having opposing sides, wherein the number of micro-machined vias includes a number of salicided electrical connections;

coupling a number of semiconductor chips to a first side of the silicon interposer;

coupling a number of semiconductor chips to a second side of the silicon interposer; and electrically coupling the at least one of the number of semiconductor chips on the first side of the silicon interposer to at least one of the number of semiconductor chips on the second side of the silicon interposer using the number of salicided electrical connections.

22. The method of claim **21**, wherein forming a number of micro-machined vias through a silicon interposer having opposing sides includes forming the number of micro-machined vias through a silicon interposer formed from recycled silicon wafers.

23. The method of claim **21**, wherein coupling a number of semiconductor chips to a first side of the silicon interposer includes coupling at least one active circuit to the first side of the silicon interposer.

24. The method of claim **21**, wherein coupling a number of semiconductor chips to a second side of the silicon interposer includes coupling at least one passive circuit to the second side of the silicon interposer.

25. The method of claim **21**, wherein the method further includes coupling a capacitor to the second side of the silicon interposer.

26. A method for forming an electronic system module, comprising:

forming a number of micro-machined vias through a silicon interposer having opposing sides, wherein forming the number of micro-machined vias through the silicon interposer includes forming salicided connections in the number of micro-machined vias;

coupling at least one semiconductor chip to a first side of the silicon interposer;

coupling at least one semiconductor chip to a second side of the silicon interposer; and

electrically coupling the at least one semiconductor chip on the first side of the silicon interposer to the at least one semiconductor chip on the second side of the silicon interposer using the number of micro-machined vias.

27. A method for forming an electronic system module, comprising:

forming a number of micro-machined vias through a silicon interposer having opposing sides, wherein the number of micro-machined vias includes a number of salicided electrical connections;

coupling at least one active circuit to a first side of the silicon interposer;

coupling at least one passive circuit to a second side of the silicon interposer; and

electrically coupling the at least one of the number of semiconductor chips on the first side of the silicon interposer to at least one of the number of semiconductor chips on the second side of the silicon interposer using the number of salicided electrical connections.

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