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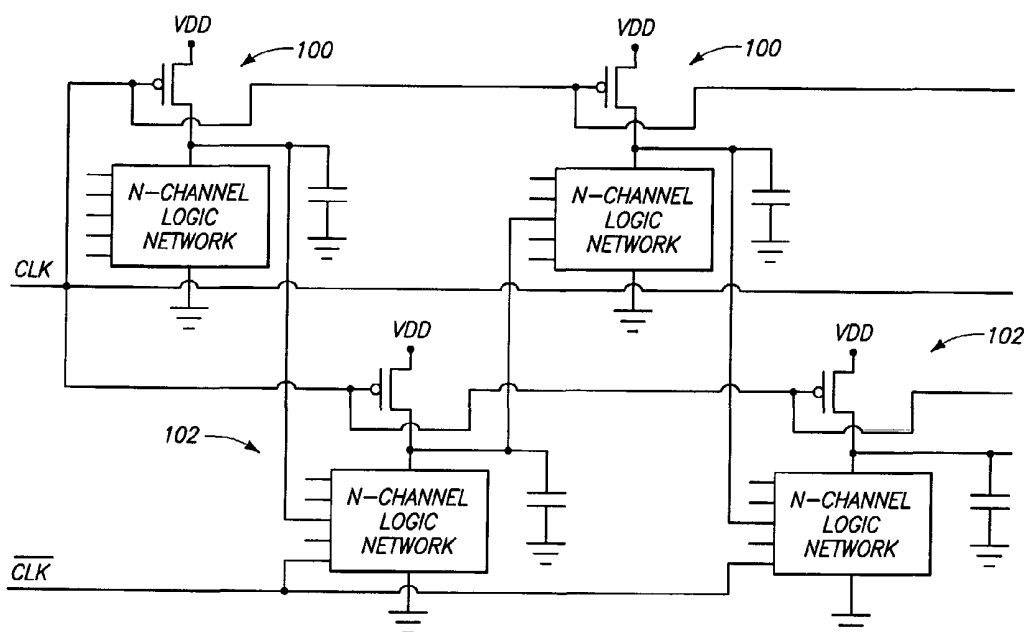
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(54) Title: MONOTONIC DYNAMIC-STATIC PSEUDO-NMOS LOGIC CIRCUIT AND METHOD OF FORMING A LOGIC GATE ARRAY



(57) Abstract: A monotonic dynamic-static pseudo-NMOS logic circuit comprises a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input; and a static logic circuit having a clock bar input and having an output configured to be precharged low when a high value of the complement of the clock signal is provided to the clock bar input. A logic gate array comprises a plurality of vertical ultrathin transistors coupled together.



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