

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
10 October 2002 (10.10.2002)

PCT

(10) International Publication Number
WO 02/080227 A2

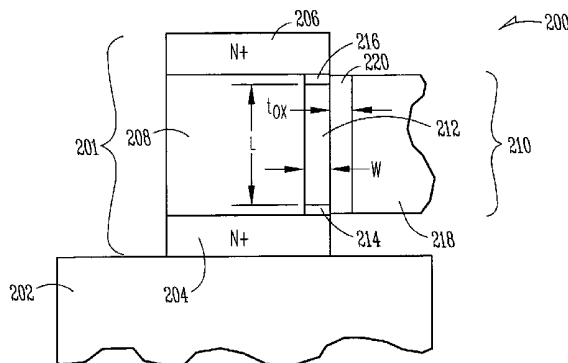
- (51) International Patent Classification⁷: H01L (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.
- (21) International Application Number: PCT/US02/03311
- (22) International Filing Date: 6 February 2002 (06.02.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 09/780,144 9 February 2001 (09.02.2001) US
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- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Published:
— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MEMORY ADDRESS AND DECODE CIRCUITS WITH ULTRA THIN BODY TRANSISTORS



(57) Abstract: A decoder for a memory device is provided. The decoder array includes a number of address lines and a number of output lines. The address lines and the output lines form an array. The decoder includes a number of vertical pillars extending outwardly from a semiconductor substrate at intersections of output lines and address lines. Each pillar includes a single crystalline first contact layer and a second contact layer separated by an oxide layer. The decoder further includes a number of single crystalline ultra thin vertical transistor that are selectively disposed adjacent the number of vertical pillars. Each single crystalline vertical transistor includes an ultra thin single crystalline vertical first source/drain region coupled to the first contact layer, an ultra thin single crystalline vertical second source/drain region coupled to the second contact layer, and an ultra thin single crystalline vertical body region which opposes the oxide layer and couples the first and the second source/drain regions. A plurality of buried source lines formed of single crystalline semiconductor material are disposed below the pillars in the array for interconnecting with the first contact layer of pillars in the array. And, each of the number of address lines is disposed in a trench between rows of the pillars for addressing the ultra thin single crystalline vertical body regions of the single crystalline vertical transistors that are adjacent to the trench.



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